

STEREO IMPACT Technical Progress Report

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Subject: IMPACT Monthly Technical Progress Report, Contract NAS5-00133

Lil:

Enclosed is the monthly technical progress report for the STEREO IMPACT project for the month of January 2004.

Sincerely,

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CC:

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IMPACT Team

STEREO IMPACT Technical Progress Report

1. IMPACT Overview

This report is presented in sections by institution. Section 1 is an IMPACT Project Manager / System Engineer's overview.

1.1. Contracting / Funding

Funding through February has been received. Because of pipe-line delays in the system through to the subcontractors (Caltech and UMD) it is important that IMPACT be funded somewhat in advance of expected spending.

1.1.1. Liens

This is a list of Liens. Liens for activities at other institutions are sometimes repeated in their subsections of this report. These liens are estimated additional costs that might be incurred if problems happen. Only problems with a significant likelihood of occurrence are tracked. These liens are usually associated with risks in the risk list (see section 1.5), and you can see the predicted likelihood of occurrence there. Some of these liens have been requested to be encumbered by Project, marked (*).

UCB:

No.	Cause	Amount	Date
1*	LVPS schedule delays extend manpower (Risk UCB29). Cost a 1-month delay at full LVPS team spending rate.	\$35,000	01/04
2	Late failure in thermal vac requires rework/retest (Risk UCB27, etc).	\$30,000	02/04
3	Testing failure requires rebuild/retest a board (using existing spare parts)	\$20,000	~02/04
4	EMC rework and retest required (Risk UCB11). Assume rework can be done in a week or two.	\$30,000	05/04
5	Schedule delays cause the consumption of boom suite schedule contingency (various risks). Cost 35 days of contingency at UCB I&T team rate.	\$50,000	07/04
6	STE calibrations sources. \$12,500 Quote is over the earlier ROM of \$10K.	\$2,500	11/04
7	SEP Thermostats. These were over the budgeted amount. Budget was \$10K at Caltech. Parts were actually \$21,200, paid by UCB (for now Caltech will hold the \$10K against other liens)	\$11,200	11/03

Caltech:

No.	Cause	Amount	Date
1	Budget does not contain funding for investigations of part failures or contamination failures, re-makes of boards if coupons fail, etc. Some of this has already occurred, as more rework has been required in the hybrid development area than we budgeted for. Some die have failed test, some units have failed PIND testing, and in a couple of cases leaks have occurred after lead bending, which was caused by a problem	\$50,000	03/04

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	with the tooling that has been corrected. In addition, QA costs have been a far bigger percentage of the overall cost than anticipated. Currently the yield of hybrids has improved with 16 of 20 passing electrical test in the last batch. (Amount = ~\$50,000 (guess); Probability = 100%; time frame = March 2004).		
2	Unfunded schedule reserve: ~\$25,000. This is becoming a reality, as our latest schedules show delivery in September 2004 (as required), whereas we had budgeted for delivery in July 2004. (Amount = \$25,000; Probability = 100%; time frame = August 2004).	\$25,000	8/04
3	Possible under-budgeting of environmental testing and bake out. \$100K has been allocated. However, recent estimates suggest that the thermal balance/thermal vacuum test may require about 3 weeks. Recent cost estimates at JPL suggest that that might take the entire \$100K. We are investigating other places for the environmental test program where the costs may be less. (Amount = ~\$50,000 (guess); Probability = 50%; time frame = July 2004).	\$50,000	7/04
4*	GSE Software support (extend a few months after January 2004)	\$60,000	1/04
5*	Engineering Assistant (Risk UCB033)	\$24,000	1/04
6*	Engineering support to maintain schedule (Risk UCB033)	\$63,000	1/04
7*	Technician Support to maintain schedule (Risk UCB033)	\$38,000	1/04
8	Overlooked hybrid costs: it was not realized that the cost estimate we were given for the hybrids did not include the qualification costs of 10 units. We have asked for a quote from JPL. (Amount = ~\$10,000 (guess); Probability = 100%; time frame = March 2004).	\$10,000	3/04
9	Unbudgeted tests: there are a number of tests outlined in the STEREO/IMPACT Requirements Verification Matrix that we are listed as responsible for but for which we did not budget. (Some I wasn't aware of and some I mistakenly thought would be done at UCB as part of EMC testing.) Test plans and procedures will need to be written and existing instrumentation either calibrated or new instrumentation obtained. These include requirements 4.10, 4.12, 4.23, 4.27, 4.28, and 4.42. If we have to get JPL to help us, the cost could be significant. (Amount = ~\$25,000 (guess); Probability = 50% (UCB might help us); time frame = July 2004).	\$25,000	7/04

UMd:

No.	Cause	Amount	Date
1	SIT foils fail acoustic test	\$20,000	2/04
2	SIT Vibration (currently planned to be combined with HET	\$15,000	2/04

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	instruments, but may not work out)		
3	Parts screening (some parts not yet Oked by PCB and may need addition screening)	\$10,000	9/03
4	Particle Calibration at BNL. This is desired but not required.	\$20,000	11/03
5*	Engineering Support to maintain schedule (Risk UCB033)	\$60,000	1/04

GSFC (Tycho):

No.	Cause	Amount	Date
1	Revise SEP Central/LET/HET vibration analysis if required	\$5,000	11/03
2*	Extra Solid-state Detector Lab manpower support to accommodate late detector delivery (Risk UCB033)	\$20,000	12/03
3	Travel for accelerator end-to-end test	\$5,000	12/03?
4	Tom Nolan flight software support (Risk UCB033)	\$15,000	2/04
5*	Engineering support to maintain schedule (Risk UCB033)	\$40,000	1/04
6			

1.2. **Significant System-Level Accomplishments**

- Held the IMPACT PER at UCB in preparation for the first environmental tests (SEPT)
- Participated in Project EMC committee meeting
- Had a number of meetings/telecoms to plan the thermal vac and bakeouts for IMPACT with Contamination Control personnel.
- Final SEP ETU get-together closed out remaining issues.

1.3. **System Design Updates**

- None

1.4. **System Outstanding Issues**

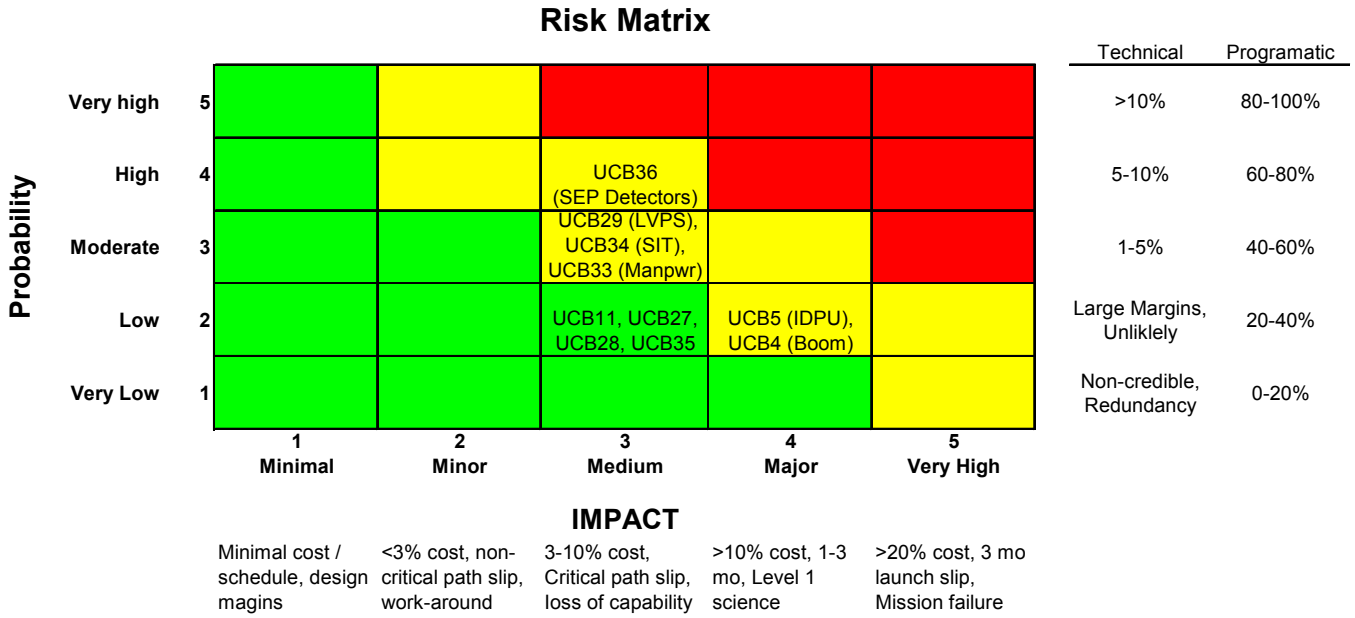
- IMPACT harness shielding waiver approved by EMC committee, pending CCB approval
- SWEA door activation transient waiver approved by EMC committee, pending CCB action.
- SWEA VMI Multiplier MRB pending test results (PFR 6001)
- A number of waivers against the environmental test specification need to be submitted.

1.5. **Top 10 Risks**

Top 10 risks are attached. The HET/LET/SIT detector fallout problem is new to the list. The probability of a significant schedule problem as a result is high unless we come up with a work-around. We are waiting to hear from the manufacturer on how soon we can get replacement detectors before we decide on a new plan. The new plan is likely to involve starting environmental tests with poor detectors and replacing them later.

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IMPACT Top Ten Risks 2/2004



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No.	Risk Item	Score	Mitigation	Mitigation Schedule			
				Sub-system Test	System Test	Env test	Early Orbit Test
UCB_5	IMPACT boom is a new design. Failure could affect Imager pointing requirements as well as boom-mounted instruments.	MEDIUM	Design for reliability. Early prototype testing. Qual model testing completed. Adequate force margins demonstrated.	MEDIUM	MEDIUM	MEDIUM	LOW
UCB_4	The IDPU is a single point failure mechanism for the IMPACT suite and PLASTIC	MEDIUM	IDPU is a simple, reliable system. Extra attention has been paid to ensuring its reliability, minimizing the risk of fault propagation. Extensive EM & FM testing	MEDIUM	MEDIUM	MEDIUM	MEDIUM
UCB_36	HET, LET, and SIT detector fallout during life test. Not enough HET detectors for the flight build, and few or no spares for SIT and LET. New detectors being obtained, but there is a schedule risk	MEDIUM	Prep for early delivery of replacement detectors. Proceed with poor detectors and replace them with new ones later in the schedule	MEDIUM	MEDIUM	MEDIUM	LOW
UCB_34	SIT Schedule slippage, on critical path	MEDIUM	Add manpower to recover schedule	MEDIUM	LOW	LOW	LOW
UCB_29	LVPS behind schedule, on critical path; further slipping could delay delivery to spacecraft	MEDIUM	Add manpower to LVPS task to avoid further slippage	MEDIUM	LOW	LOW	LOW
UCB_33	Instrument fabrication & test schedule limited by available personnel	MEDIUM	Subcontract assembly work, authorize overtime, bring on new people	LOW	LOW	LOW	LOW
UCB_35	New undiagnosed Actel part failures may impact flight hardware	LOW	Keep abreast of Actel's analysis results; Make changes to minimize ground bounce which may be related to failures according	LOW	LOW	LOW	LOW
UCB_11	Stringent EMI requirements may delay schedule if testing fails	LOW	Careful design, ETU power converter testing, early system testing	LOW	LOW	LOW	LOW
UCB_27	Actel timing differences between flight & ETU parts may cause failures late in testing impacting delivery schedule	LOW	Do FM Thermal Vac early to allow time for finding and fixing timing problems; for designs on the critical path, consider installing a flight Actel in the ETU &	LOW	LOW	LOW	LOW
UCB_28	Thermal limitations of detectors result in a low bakeout temperature which might require a very long bakeout	LOW	Bakeout subsystems prior to detector integration to reduce time of instrument-level bakeout; early bakeout	LOW	LOW	LOW	LOW

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2. Berkeley Status

2.1. *Summary of Status*

Schedule status through January has been provided separately.

2.2. *Major Accomplishments*

SWEA/STE:

- SWEA/STE flight boards ready to load.
- First STE flight Preamp board loaded and tested
- STE flight detector boards have detectors mounted, in test.
- STE, SWEA Pedestal, and STE-U preamp housing fabrication complete
- STE doors out to get calibration source applied

IDPU:

- DCB flight units passed final inspection.
- IDPU Comprehensive Performance Test procedure complete, run on ETU
- Working on software Build 3 for IMPACT.
- PLASTIC software Build #2.3 tested with PLASTIC ETU at UNH; Next builds planned.

LVPS/HVPS:

- SIT HVPS FM #1 delivered to UMd for test with instrument.
- SWEA/STE-D LVPS PWB ready to load.
- PLASTIC LVPS assembly complete, in test.
- SEP boards being loaded; first of three boards in the FM1 supply completed and in test.
- IDPU LVPS board out to fab (this is the last of the UCB PWBs).

Boom:

- Flight parts are in (a few failed inspection and had to be returned for rework).
- Assembly has started. Most tubes are glued to their rings.

GSE:

- Last Science GSE (SWEA) in progress.

2.3. *Design Updates*

- None.

2.4. *Outstanding Problems*

2.5. *New Problems*

2.6. *Top Risks.*

- LVPS schedule tight
- Open Actel problems

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2.7. *Problem/Failure Quick Look*

ID #	Description	Assignee	Opened	Closed
1001	Qual boom deployment failure in Thermal Vac	McCauley	2003-08-15	2004-01-07

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3. GSFC (SEP) Status

STEREO/IMPACT/SEP/GSFC Progress Report for January, 2004 – (von Roseninge, Baker, Hawk, Shuman, Nahory, Wortman)

3.1. *Summary of Status*

The current delivery dates of the HET flight units to Caltech are 28 May and 21 June of 2004. This change resulted from the recent rescheduling exercise.

3.2. *Major Accomplishments*

- Worked on schedule restructuring for re-baselining STEREO Project level schedule.
- Our first flight detectors for the HETs have been received and are under test: 9 H1 detectors and 10 H3 detectors. Of these, 8 H1 detectors and 7 H3 detectors have been in a thermal-vacuum test for 3 weeks. Approximately 2 out of 3 detectors show growing leakage current as a function of time. Discussions have begun with Caltech and Micron as to what to do about this. We are assessing the need to order additional detector mounts so that Micron can make additional detectors. We have also advised Micron of the problem with growing leakage currents. Micron is about to receive over 30 new polished wafers and will start to make additional detectors. In addition, they have 10 more H3 detectors which they will be shipping very soon. We require 4 H1 detectors and 14 H3 detectors for the flight units.
- Thermal vacuum testing of 5 SIT detectors has also been underway. Two of the 5 detectors look very good, whereas the remaining 3 are bad. Two are required for flight. One of the 3 bad detectors is still under warranty. Ortec, the detector manufacturer, is being contacted to provide us with at least one working spare.
- A possible solution to a concern with respect to aerodynamic heating immediately after fairing release was investigated by John Hawk. By using a double foil window on LET instead of a single foil, the temperature of the affected LET detectors will rise from 20 degrees C to 30 degrees C instead of to 45 degrees C, a substantial and sufficient improvement. The double window will raise the threshold energy of LET somewhat above the level of its scientific requirements, so a waiver request has been filed to permit the double window.
- The HET flight model 1 PC board is fully populated except that a socket has been substituted for the flight Actel. Additional changes to the Actel design are being investigated to respond to concerns which have been recently raised regarding ground-bounce problems in the flight Actels for both HET and SIT. The HET board has now been thoroughly checked out so, when we finally are able to mount a flight Actel, we will be reasonably certain that any problems which we see are related to the flight Actel and not to other parts of the HET board. At present, we envision that the socket will be replaced by a flight Actel in about 2-3 weeks. The flight Actels do not fit into the socket.

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- A design change was requested by UMD for the SIT Actel to ensure that the SIT High Voltage is truly OFF at turn-on. This was fairly easy to implement since the Actel ground-bounce problem had held back burning of the flight Actels.
- Population of the SIT energy board is essentially complete except for some final parts which are about to be delivered.
- The HET ETU was sent to Caltech for tests of the full-up engineering system (minus SEPT, but including the IDPU). This was a follow-up to a previous test in which we encountered some problems with on-board code uploads to E2PROM and to RAM. The earlier problems have now been resolved.
- The SIT thermal vacuum and thermal balance tests have been shifted from Caltech to GSFC. The SEPT thermal balance test will also be performed at GSFC.
- Reconfigured SIT back plane per Uof Md. changes and finalized back cover of electronics to conform to new layout.
- Worked on designs for HET Telescope.
- Worked on configuration changes for SEP-LVPS housing after receiving boards from Berkeley.
- Completed thermal heater design for SEPT and SIT and submitted for quote to vendors.

3.2.1. Next Month-

- Fabricate some preliminary LET foils for test.
- Complete HET on-board software specifications.
- Cross-check drawings and SIT ETU parts;
- Complete changes to Actels re ground bounce issue.
- Continue testing flight detectors for HET and SIT.
- Update ICD with APL to include mounting hole diameters and correct LET FOV.
- Update mass of SEP Main.
- Work on defining the HET and SEPT radioactive sources to be supplied by GSFC.
- Close out remaining RFAs from CDR.

3.3. ***Design Updates***

Work being shifted from UofMD and from Caltech will require some additional funding; this was included in the recently re-baselined budget.

3.4. ***Outstanding Problems***

See previous discussion of the LET aerodynamic heating issue.

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3.5. ***New Problems***

- HET detector leakage currents growing in vacuum. Only 2 good SIT detectors. See previous discussion.
- Continued slow schedule slipping. This has been addressed in the re-baselined schedule.

3.6. ***Top Risks***

Inadequate numbers of good HET detectors. The whole HET telescope can easily be retrofitted late in the game if necessary.

3.7. ***Problem/Failure Quick Look***

4. Kiel/ESTEC (SEPT) Status

January 2004

4.1. Summary of Status

- a) All SEPT mechanical components which received thermal coating at GSFC are returned to Kiel.
- b) New schedule for environmental tests established for February and March 2004.

4.2. Major Accomplishments

- a) Assembly of electronics for FM2 complete. Electronics test complete. Delivery to Kiel complete.
- b) Final integration of all four flight units finished.
- c) Electronics calibration and calibration with radioactive sources and muons ongoing.
- d) Functional tests, pinpuller activation of door mechanisms ongoing.
- e) MLI fit check with engineering model blankets.
- f) Participation in Pre-Environmental Test Review at UoB.
- g) Participation in Bake-out meeting at UoB.
- h) Responding to request for actions from PER and Bake-out meeting.
- i) Preparations for vibration and TV test ongoing.
- j) PDFE lot acceptance test (LAT) passed.

4.3. Design Updates

4.4. Outstanding Problems

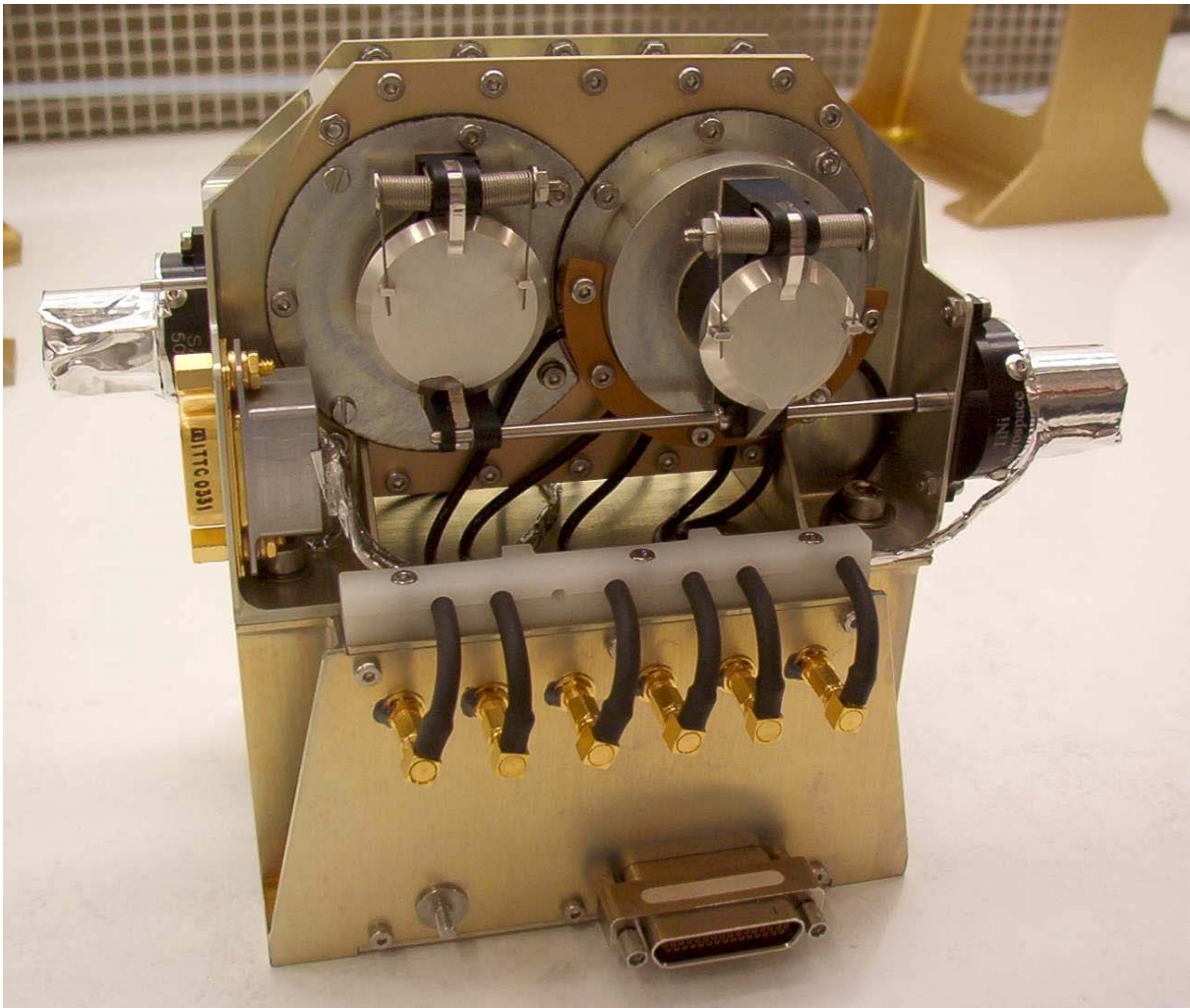
4.5. New Problems

Mechanical interference of EM MLI blanket with door mechanism. Cause: structural model used to tailor blanket did not show subtle details of opening mechanism. Solution: use SEPT-EM when tailoring flight blankets.

4.6. Top Risks

4.7. Problem/Failure Quick Look

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SEPT Flight Unit ready for test

5. Caltech/JPL (SEP) Status

5.1. Summary of Status

Activities centered on the detector development, electronics development, and flight and GSE software development.

Major Accomplishments:

- Enough LET flight detectors have been tested to populate both flight sensors.
- Space Instruments, Inc. finished testing of SEP Analog/Post-Reg flight boards S/N 1 & 2 at room, hot, and cold temperatures. Both boards performed to spec.
- Final EM test (everything except for SEPT) was conducted successfully.

Critical Milestones status:

- Milestone 18 (HET-All Flight Detectors Received) has not been accomplished. All HET detectors should be received by sometime in February 2004.
- Milestone 19 (LET-All Flight Detectors Received) was accomplished. However, note that leakage current growth problem will mean some detectors will be replaced under warranty.
- Milestone 20 (SEP Package-EM I&T Complete) was accomplished.

Detectors:

- Micron Semiconductor has delivered all of the L1, L2, and L3 detectors for LET, as well as all of the H1 and half of the H3 detectors for HET. At the end of December Micron was testing the remaining HET detectors with a goal of delivering them in the first half of February.
- Detector testing at Caltech has progressed to the point that sufficient flight-quality devices to fully populate both of the flight LET instruments have been identified. Additional testing is proceeding and will allow us to identify a pool of flight-quality LET spare detectors.
- As previously reported, thermal-vacuum testing of L3 detectors at Caltech identified long-term leakage-growth problems in 6 of 11 detectors tested. Some preliminary investigation of this problem indicated that it is apparently associated with an instability of the detector breakdown voltage in vacuum. Further studies to characterize this problem are planned.
- Initial vacuum tests of H1 and H3 detectors at GSFC are indicating that some of those devices (which are made from the same type of silicon wafers as the L3 detectors) are similarly affected. This problem has been discussed with Micron in order to jointly work out a plan for production of some replacement detectors. Anticipating this possibility, Micron has ordered additional 1-mm-thick polished silicon wafers (approximately 30 slices) that could be used for making replacement detectors. They are expecting to receive them during the first half of February.

Electronics:

- The design of the SEP Central MISC Actel was finalized, incorporating a 10 nsec delay for half of the address and data lines to mitigate ground bounce. The mitigation was verified to reduce the worst-case ground bounce amplitude by a factor of two from 400 mV to 200 mV as measured at a particular witness pin for the commercial parts. The worst-case bounce occurs when the data lines all switch from high to low

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simultaneously. The witness pin was located near the bank of data lines but not in the midst of the bank, so the peak magnitude of ground bounce within the Actel gate array directly behind the bank of data lines is expected to be larger than the 400 and 200 mV measured at the witness pin. In the final design all unused i/o pins were programmed as low-driven outputs, providing additional pins for use as witness pins, some located near the center of the data line bank. Peak ground bounce among these pins was found to be 500 mV for the commercial part. (SPICE simulations are needed to infer the internal ground bounce amplitudes given the witness pin measurements. A request for help in getting the needed SPICE model parameters for the internal ACTEL power and ground grids and package pins was made to Rich Katz, but no reply was forthcoming. Any help with this request would be appreciated. Recall that ground bounce is one theory for the damage of our earlier failed Actel FPGA.)

- A flight Actel FPGA has been programmed for SEP Central. It will be mounted soon on the flight SEP Central Logic board and tested. The board itself now has a socket for a commercial Actel FPGA and has been partially verified. The FORTH system has been successfully loaded into EEPROM and booted. Prior to programming the flight ACTEL, a commercial part with identical routing was tested in our EM board over temperature from about -35 C to +60 C. Actel TIMER software was used to verify setup and hold timing margins.
- The second pre-integration check occurred using engineering models for all instruments and SEP Central boards except for SEPT. Problems identified in the first EM get-together were verified as solved, including checksum errors during binary uploads and local and remote commanding through the GSE. The SEP Central MISC was verified to boot itself and HET, LET, and SIT at power up, using binary code stored in the SEP Central EEPROM. Booting from the alternate EEPROM bank was also verified. (SEP Central contains two banks of EEPROM, each capable of storing a complete copy of all HET, LET, SIT and SEP code.) The "partial" boot method in which SEP Central boots itself but not the instruments was also verified. It was also verified that tables that define instrument operation could be loaded either directly to the instrument RAM or to EEPROM within SEP Central. The outline of a formal checkout procedure was made.
- Progress continued on LET flight software, with a second version of Andrew Davis' routine being delivered to Rick Cook. Andrew will deliver a 3rd version within about one week, and that version will be the first to be entirely integrated and should contain implementation of all features.
- Space Instruments, Inc. finished testing of SEP Analog/Post-Reg flight boards S/N 1 & 2 at room, hot, and cold temperatures. Both boards performed to spec and were delivered back to Caltech for further integration.
- Finished assembly of SEP Logic flight boards S/N 1 & 2 at Caltech. Both boards have a socket for testing with EM Actel prior to installing the flight part.
- Bias Supply flight boards S/N 1 & 2 assembled at GSFC and delivered to Caltech. We have decided on temporary bias voltage settings in order to proceed with testing of the boards and will install select resistors for those values prior to sending the boards to Space Instruments, Inc.
- Kitted flight parts for LET boards and will send them to GSFC for assembly in early February. The assembly is supposed to take about three weeks.

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- Received a new batch of flight PHASIC hybrids from JPL and will start a 9.2-day burn-in test on 18 units in early February. Expect to finish functional testing and selection of flight parts by the end of February.
- Received composite backshells from Glenair and delivered them to JPL for final assembly and termination of SEPT/SIT flight harnesses.

Software (Davis):

- Completed and delivered second fully-featured and working version of LET event processing software to Rick Cook.
 - fixed various bugs found during testing
 - improved logic to handle events with multiple hits
 - re-arranged variables and tables in memory to be compatible with Rick Cook's software
 - implemented some performance optimizations
 - wrote and tested code to format events for telemetry
- Continued with further testing of the current version using simulated events, including various kinds of odd, malformed, and multiple-hit events.

GSE:

- Support for SEP EM test: This month there was a hardware test involving SEP Central, LET, SIT, and the IMPACT IDPU. In support and in conjunction with that test the activities below were performed.
 - Modification of the GSE software to upload data to the EEPROM to the SEP sensors. This was done to accommodate a change in the SEP on-board software.
 - Modified and tested command communications (via SCMs) between the SEP GSE and the HET and SIT GSEs. All command communication appears to be working properly. We tested all expected modes of command communications between the GSEs.
 - Modified and tested command communication between the SEP GSE and the IMPACT GSE. Command communication appears to work properly, and all modes of command communications were tested between the GSEs.
 - Tested the booting of the SEP sensors via commands from the IMPACT IDPU forward from the SEP GSE.
 - Telemetry communications between the GSEs remained stable.
- Began writing software to display rates from the new LET telemetry format.

5.2. *Design Updates*

- No resource updates this month.

5.3. *Outstanding Problems*

- The problems with the two flight ACTELs are being investigated by ACTEL and by Rich Katz at GSFC.
- Higher than expected thermal vacuum run failures of the L3 detectors will require Micron to provide a few additional flight devices.
- Preliminary analysis suggests that the nominal fairing release time will cause excessive heating to the L1 detectors (to 65C) based on the heating levels specified, which may have considerable margin (factor 3) over what might actually be

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experienced. The lower heating level would only heat the detectors to 45C. In the meantime, partly for other reasons, an additional window is being added to LET and perhaps that will mitigate the problem. More calculations are underway.

5.4. ***New Problems***

- Leakage current growth problem in thermal vacuum testing of 1-mm devices is being investigated.

5.5. ***Top Risks.***

- ACTEL parts may not be reliable. This would affect many NASA projects.
- 1-mm detectors may have a serious leakage current growth problem. However, enough good LET detectors have been identified to populate both flight instruments. HET detectors may be more of a concern, perhaps requiring swapping out detectors later than desired.
- Higher than expected free molecular heating might require a re-design of the LET sensor head.
- The budget is very tight with no reserve being held at Caltech.

5.6. ***Problem/Failure Quick Look***

- None.

5.7. ***Lien List***

- Budget does not contain funding for investigations of part failures or contamination failures, re-makes of boards if coupons fail, etc. Some of this has already occurred, as more rework has been required in the hybrid development area than we budgeted for. Some die have failed test, some units have failed PIND testing, and in a couple of cases leaks have occurred after lead bending, which was caused by a problem with the tooling that has been corrected. In addition, QA costs have been a far bigger percentage of the overall cost than anticipated. Currently the yield of hybrids has improved with 16 of 20 passing electrical test in the last batch. (Amount = ~\$50,000 (guess); Probability = 100%; time frame = March 2004).
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done at UCB as part of EMC testing.) Test plans and procedures will need to be written and existing instrumentation either calibrated or new instrumentation obtained. These include requirements 4.10, 4.12, 4.23, 4.27, 4.28, and 4.42. If we have to get JPL to help us, the cost could be significant. (Amount = ~\$25,000 (guess); Probability = 50% (UCB might help us); time frame = July 2004).

6. SIT MONTHLY TECHNICAL PROGRESS REPORT

January 2004

6.1. SUMMARY of STATUS

- a. SIT TELESCOPE – Prototype at GSFC for assistance in building flight units. Flight SSDs are under test at GSFC.
- b. SIT TOF System - FM1 was downgraded to ETU and is part of the ETU electronics under test at UMd. Work is proceeding at MP Ae to generate a new FM1 and FM2.
- c. SIT Energy System – ETU is integrated in the ETU electronics at UMd. Flight units are under construction at GSFC.
- d. SIT Logic System – The updated ETU logic board and updated motherboard have been integrated with the remaining electronics. Testing is underway at UMd.
- e. SIT HVPS - Flight HVPS FM1 is undergoing test at UMd.
- f. Flight Software – Version 11/20/03 is installed in the ETU under test at UMd.

6.1.1. Schedule Changes

The current SIT schedule is available from Jim Rogers

6.2. MAJOR ACCOMPLISHMENTS

6.2.1. This Month

- ETU: The ETU was sent to Caltech for interface testing. The unit worked well. During testing we demonstrated several new capabilities including loading tables from SEP Central EEPROM, from files at Caltech and from files at GSFC. In addition, we were able to observe data and send commands from UMd.
-
- Logic Board: The logic board fabrication was delayed while we decided how to proceed with the Actel ground bounce problem. It was decided to apply the Caltech-invented solution of delaying alternate output pins in several banks by about 10 nS to prevent adjacent pins from changing state at the same time. We decided not to change the pinout as this would require an extra cycle of ETU board layout and test before we built the flight board and the schedule is too tight for this. George Winkert at GSFC is in charge of reworking the Actel to accomplish the output delays. A non-flight Actel will be generated and tested in the existing ETU before burning the flight Actel.
- Energy board: Fabrication was begun at GSFC. It could not be completed because of several small issues of hole size which are being resolved. We are currently waiting for new coax terminators to replace the originals which had gold plating problems.
- ATOF Board – Construction and testing is proceeding on both ATOF and DTOF flight TOF boards.
- Telescope: The prototype telescope was turned over to GSFC to be used to check design documents and to document assembly procedures. We expect it back in mid-February to be re-integrated with the ETU. The solid state detectors are undergoing thermal-vacuum testing at GSFC. There is indication of excess current in several of

STEREO IMPACT Technical Progress Report

the detectors. We need to keep a close eye on this and be prepared to purchase another SSD if necessary to maintain three working units (2 flight, one flight spare).

- HVPS – Testing was begun after the vacuum chamber was repaired, but was interrupted by ETU testing at Caltech. Some pickup was noted on the control line from the sync line preventing the supply from achieving the expected voltages. We are changing cabling to try to fix this.

6.2.2. Next Month

Next month we will (God willing) receive the assembled energy boards for trimming, and the flight TOF boards for testing. The motherboard and logic board designs will be released for flight PCB fabrication.

6.3. **DESIGN UPDATES**

6.4. **Resources**

	Last Month	This Month	Change
Mass (kg) *	1.46	1.46	0
Power (W)	1.56	1.56	0.0
Telemetry (bps)	418	418	0

* Includes 200g book-kept by GSFC for SIT structure

A new estimate of Actel power for the flight units indicates that power will increase. Previous estimates had neglected the effect of the triple gates in the flight units for single-event upset protection.

6.5. **OUTSTANDING PROBLEMS**

We are continuing to work Energy parts issues.

6.6. **NEW PROBLEMS**

Actel ground bounce problem.
Excess current in as many as three of our SSDs.

6.7. **NEW RISKS**

6.8. **PROBLEM/FAILURE QUICK LOOK**

Starts at first turn-on of flight hardware.

ID #	Description	Assignee	Opened	Closed

7. CESR (SWEA) Status

CESR- TOULOUSE- France

Author : Claude Aoustin / Project Manager

SWEA PROGRESS REPORT # 28 (February 11, 2004)

January 2004

CESR is in charge of :

- Electrostatic analyzer with deflectors, grids and Retractable Cover
- Detector consisting of two MCP rings
- Amplifiers and discriminators
- 3 High voltages

7.1. *Summary of Status*

7.1.1. ETU1

Delivery to UCB was planned for 12/07/2002 : done 26/09/2002

7.1.2. ETU2

Mechanical fabrication 100 % done
Integration done for the vacuum test configuration.
Electronic boards tested (100 %).

7.1.3. FM1 / FM2

Mechanical fabrication 100 % done.
Electronics boards fabrication : 100% done

7.2. *Major accomplishments*

7.2.1. FM1 :

Delivered to SSL : 8 December 2003.

7.2.2. FM2 :

FM2 integrated in 2 parts :

- bottom with the inner sphere ready for MCP characterization test
- top with grids, external sphere and pin puller.

We have got some delay on the availability of the vacuum chamber. Calibrations will start only mid March and will be finished in the second half of April.

Delivery to SSL UCB by end of April.

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7.3. **Design Updates**

Mass : 967 g (EM is 950g without cover opening mechanism)

Power : 446 mW min ; 662 mW max

7.4. **Outstanding Problems**

- HV resistors life test 1000 h. finished. Good results.
- LT1024 radiation test performed by GSFC. It shows drift of the bias current. This has an impact on the deflectors HV. The 1 Mgohms resistors R18 and R31 have been changed by 5.1 Mgohms resistors. This is minimizing the impact of the radiation and is acceptable for the science data quality up to 12 krads. Furthermore a sheet of 1mm of copper has been added on the top of all the LT1024.

7.5. **New problems**

7.6. **Top Risks**

7.7. **Problem Failure Quick Look**

- HV multiplier from VMI HM 402 P 10 failed at -70°C !
- Problem Failure report 6001 updated by Dave.
- Failure analysis done by GSFC. It is showing a bad bonding inside the component.
- Two parts from the same lot sent to Lilian for testing.

8. GSFC (MAG) Status

There have been some QA issues with the MAG boards, in particular with conformal coating. The MAG heater boards have been conformal coated and are being evaluated to see if they can be used as is. The front end boards have been calibrated and are waiting to be coated once a conformal coating plan has been developed. The new MAG heater filter boards are due soon. These issues are delaying delivery of the MAG units to UCB for integration. MAG will get onto the boom suite critical path if they cannot be delivered by early April. We are working hard to avoid that.

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9. EPO at UCB

Monthly E/PO Report

January, 2003

Formal Education:

We continued to prepare for a Space Physics Teacher Professional Development workshop held at SSL in Berkeley on February 7th after the GEMS Associate training at the Lawrence Hall of Science.

Informal Education:

We worked with Dr. Bale of the STEREO-SWAVES team and the University of California music department, in particular the Center for New Music and Audio Technologies (CNMAT), to determine how to start our collaboration to map data to music in a meaningful and flexible way. It was determined that Dr. Bale will pay a music department graduate student, Roberto Morales Manzanara, to do the work, provide the computer, and we would provide the software needed for the task.

Cross Cutting:

L. Peticolas gave a talk at the American Meteorological Society (AMS) meeting in Seattle, WA on January 12th entitled: "Space weather education using sounds from data and visualizations from simulations" with co-authors: J. G. Luhmann, W. P. Abbett, N. Craig, B. J. Méndez, and I. Sircar. In this talk we shared how converting data to sound can be used in space science education. Delores Knipp at the Air Force Academy requested the talk in order to use some of the materials in her college level space physics course. There was a lot of interest in our project from teachers and other E/PO scientists.

We received comments on our STEREO-IMPACT E/PO proposal, reworked the budget and plans, and sent it to the proposal office for approval and then to Goddard for funding.

STEREO E/PO in general:

We began discussions with the Goddard to collaborate on the web-based project to map music to sound.

Respectfully Submitted,
IMPACT E/PO scientists Nahide Craig, Laura Peticolas