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Subject: IMPACT Monthly Technical Progress Report, Contract NAS5-00133

Lil:

Enclosed is the monthly technical progress report for the STEREO IMPACT project for the month of September 2003.

Sincerely,

David Curtis
IMPACT Project Manager
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CC:

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IMPACT Team

1. IMPACT Overview

This report is presented in sections by institution. Section 1 is an IMPACT Project Manager / System Engineer's overview.

1.1. *Contracting / Funding*

Funding through the end of FY03 is in place. Because of pipe-line delays in the system through to the subcontractors (Caltech and UMd) it is important that IMPACT be funded somewhat in advance of expected spending. We can "coast" for a month or two into FY04 with the existing funding with the understanding that we will be funded as soon as possible.

1.1.1. Liens

This is a list of Lien. Liens for activities at other institutions are sometimes repeated in their subsections of this report. These liens are estimated additional costs that might be incurred if problems happen. Only problems with a significant likelihood of occurrence are tracked. These liens are usually associated with risks in the risk list (see section 1.5), and you can see the predicted likelihood of occurrence there.

UCB:

No.	Cause	Amount	Date
1	LVPS schedule delays extend manpower (Risk UCB29). Cost a 1-month delay at full LVPS team spending rate.	$35,000	01/04
2	Late failure in thermal vac requires rework/retest (Risk UCB27, etc).	$30,000	02/04
3	Testing failure requires rebuild/retest a board (using existing spare parts)	$20,000	~02/04
4	EMC rework and retest required (Risk UCB11). Assume rework can be done in a week or two.	$30,000	05/04
5	Schedule delays cause the consumption of boom suite schedule contingency (various risks). Cost 35 days of contingency at UCB I&T team rate.	$50,000	07/04

Caltech:

No.	Cause	Amount	Date
1	Budget does not contain funding for investigations of part failures or contamination failures, re-makes of boards if coupons fail, etc. The amounts and timing of these types of expenditures are largely unknown. Board re-makes are in the $6,000 to $12,000 range, per board type. The budget does contain funding for board reworks, including adding haywires, etc.	$12,000	12/03
2	Unfunded schedule reserve (if we deliver in September 2004 as required rather than July 2004 as currently planned).	$25,000	8/04
3	Bakeout plans need to be firmed up. May result in more time in JPL bakeout chambers	$50,000	7/04

UMd:

No.	Cause	Amount	Date
1	SIT foils fail acoustic test	$20,000	2/04
2	SIT Vibration (currently planned to be combined with HET instruments, but may not work out)	$15,000	2/04
3	Parts screening (some parts not yet Oked by PCB and may need addition screening)	$10,000	9/03
4	Particle Calibration at BNL. This is desired but not required.	$20,000	11/03
5			
6			

GSFC (Tycho):

No.	Cause	Amount	Date
1	Revise SEP Central/LET/HET vibration analysis if required	$5,000	11/03
2	Extra Solid-state Detector Lab manpower support to accommodate late detector delivery	$20,000	12/03
3	Travel for accelerator end-to-end test	$5,000	12/03?
4	Tom Nolan flight software support	$15,000	2/04
5			
6			

1.2. *Significant System-Level Accomplishments*

- Participated in EMC Committee telecom
- Held a number of Parts Control Board meetings to review and approve parts lists for boards ready for flight build
- Performed compatibility tests between SEP ETU LVPS and SEP Central / LET ETU. Test with full SEP suite planned for October.
- Performed compatibility tests between PLASTIC LVPS ETU and PLASTIC ETU.

1.3. *System Design Updates*

- None

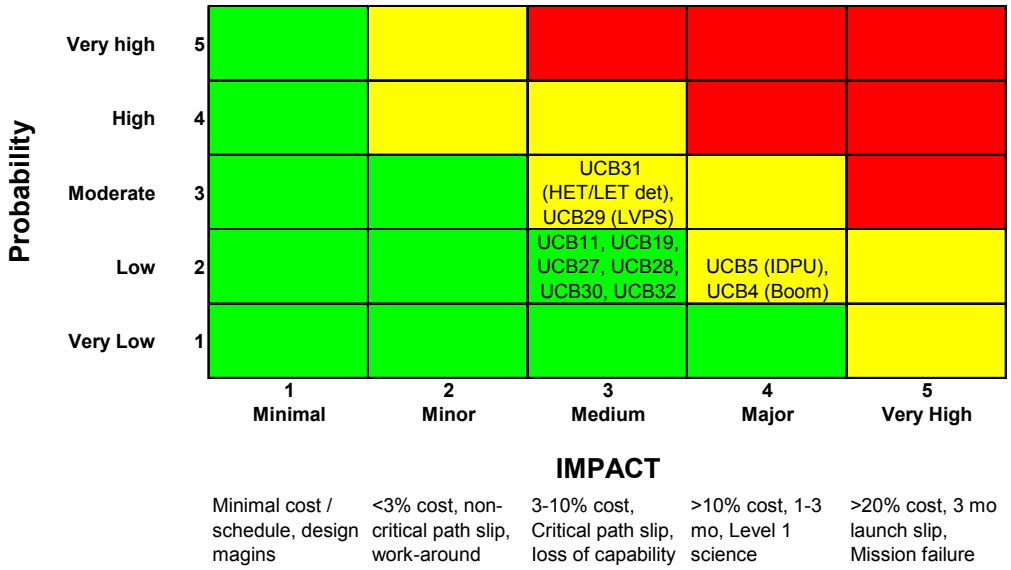
1.4. *System Outstanding Issues*

- New boom cork contamination waiver submitted, test results submitted for review.

1.5. *Top 10 Risks*

Top 10 risks are attached. No change from last month..

Risk Matrix



	Technical	Programatic
Very high 5	>10%	80-100%
High 4	5-10%	60-80%
Moderate 3	1-5%	40-60%
Low 2	Large Margins, Unliklely	20-40%
Very Low 1	Non-credible, Redundancy	0-20%

1 Minimal	2 Minor	3 Medium	4 Major	5 Very High
Minimal cost / schedule, design magins	<3% cost, non-critical path slip, work-around	3-10% cost, Critical path slip, loss of capability	>10% cost, 1-3 mo, Level 1 science	>20% cost, 3 mo launch slip, Mission failure

IMPACT Top Ten Risks 8/2003

No.	Risk Item	Score	Mitigation	Mitigation Schedule						
				PDR	EM Test	CDR	Sub-system Test	System Test	Env test	Early Orbit Test
UCB_5	IMPACT boom is a new design. Failure could affect Imager pointing requirements as well as boom-mounted instruments.	MEDIUM	Design for reliability. Early prototype testing. Qual model testing completed. Adequate force margins demonstrated.	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	LOW
UCB_4	The IDPU is a single point failure mechanisim for the IMPACT suite and PLASTIC	MEDIUM	IDPU is a simple, reliable system. Extra attention has been paid to ensuring its reliability, minimizing the risk of fault propagation. Extensive EM & FM testing	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM
UCB_31	HET/LET ETU detector mounting difficulties impacting schedule	MEDIUM	Idnetify and solve problems; bring in outside experts to evaluate process, continue with flight detector fab in parallel	MEDIUM	MEDIUM	MEDIUM	MEDIUM	LOW	LOW	LOW
UCB_29	LVPS behind schedule, on critical path; further slipping could delay delivery to spacecraft	MEDIUM	Add manpower to LVPS task to avoid further slippage	MEDIUM	MEDIUM	MEDIUM	MEDIUM	LOW	LOW	LOW
UCB_11	Stringent EMI requirements may delay schedule if testing fails	LOW	Careful design, ETU power converter testing, early system testing	MEDIUM	MEDIUM	MEDIUM	LOW	LOW	LOW	LOW
UCB_27	Actel timing differences between flight & ETU parts may cause failures late in testing impacting delivery schedule	LOW	Do FM Thermal Vac early to allow time for finding and fixing timing problems; for designs on the critical path, consider installing a flight Actel in the ETU & thermal cycle.	MEDIUM	MEDIUM	MEDIUM	LOW	LOW	LOW	LOW
UCB_28	Thermal limitations of detectors result in a low bakeout temperature which might require a very long bakeout impacting delivery schedule	LOW	Bakeout subsystems prior to detector integration to reduce time of instrument-level bakeout; early bakeout	MEDIUM	MEDIUM	MEDIUM	LOW	LOW	LOW	LOW
UCB_19	Concern about fragility of ITO surfaces required to meet ESC requirements; failure will impact SWEA science	LOW	Replace ITO with more robust solution where possible; test ITO surfaces during I&T and replace when required	MEDIUM	MEDIUM	MEDIUM	LOW	LOW	LOW	LOW
UCB_32	Parts Review Boards & Parts Waiver process could delay flight fabrication	LOW	Work to get parts lists approved, waivers into system where PCB cannot agree.	MEDIUM	MEDIUM	LOW	LOW	LOW	LOW	LOW
UCB_30	SECCHI magnetics (especially filter wheen motor) may exceed magnetics requirement, impacting MAG science	LOW	Testing completed, shielding implemented.	MEDIUM	MEDIUM	MEDIUM	MEDIUM	LOW	LOW	LOW

2. Berkeley Status

2.1. *Summary of Status*

Schedule status through June has been provided separately.

2.2. *Major Accomplishments*

SWEA/STE:

- SWEA/STE flight boards re-layed out and in review.
- STE flight Preamp board in fabrication
- STE flight detector boards in fabrication.
- STE, SWEA Pedestal, and STE-U preamp housing in flight fab

IDPU:

- Second flight DCB unit fabrication completed and passed inspection. Build cannot complete until ROM programmed and installed, which is pending final PROM software acceptance tests and ETU spacecraft interface test.
- Flight Software: PROM software acceptance test procedure completed and reviewed, ready to test. Working on Build 3 for IMPACT.
- PLASTIC software Build #2.3 near completion.

LVPS/HVPS:

- SIT HVPS FM #1 final tests delayed (engineer is sick).
- SWEA/STE LVPS in re-layout for flight
- PLASTIC LVPS ETU test complete, Layou modes complete, ready to build flight PWBs.
- SEP LVPS ETU delivered to Caltech and tested. Flight layout modifications in progress. A full up test with all the SEP ETUs scheduled for October.
- Power sequencing add to IDPU ETU LVPS and tested. Working layout modifications for flight
- There is a bottleneck in the re-layout process. Soon SEP, IDPU, and SWEA LVPS will all be in the queue. Looking for a second layout person to help out.

Boom:

- Thermal Balance test on Qual boom complete, analysis in progress.
- Most flight parts have been released and are out for manufacture. Rings are delayed pending measurements of flight tubes.
- The second batch of flight tubes was received and rejected. Have met with the manufacturer to resolve problems. Seems to be a materials problem (different batch from material used for Qual boom).
- Provided additional information for deployment failure PFR.

GSE:

- Continued additions to C&T GSE, SWEA/STE GSE.

2.3. *Design Updates*

- None.

2.4. *Outstanding Problems*

2.5. *New Problems*

2.6. *Top Risks.*

- LVPS schedule tight

2.7. *Problem/Failure Quick Look*

ID #	Description	Assignee	Opened	Closed
1001	Qual boom deployment failure in Thermal Vac	McCauley	2003-08-15	

3. GSFC (SEP) Status

STEREO/IMPACT/SEP/GSFC Progress Report for September, 2003 – (von Rosenvinge, Baker, Hawk, Reames, Shuman, Wortman)

3.1. *Summary of Status*

The current delivery dates of the HET flight units are 2/28/04 and 3/15/04. These dates were revised two months ago because: (1) problems with obtaining fully qualified detector mounts have slowed delivery of flight detectors, (2) additional time was needed to complete evaluation of the engineering electronics, (3) approval of the flight parts list has been slow, and (4) flight PHASICs will be delivered later than previously expected.

3.2. *Major Accomplishments*

The HET flight PC boards were received in mid-September and their coupons have been inspected and accepted. All parts for the HET flight boards have been approved and board population will begin soon. However questions have been raised relative to the detector connectors (e.g. solder wicking during attachment and how many mate/demates they can tolerate). A soldering test and a mate/demate test were conducted on both the HET and LET connectors. As a result, the HET connectors have been approved (SAMTEC HTS/HSS type with round pins). The LET detector connectors (SAMTEC CLT/TMM type with square pins) have an issue with removal of gold from the underlying Ni on the female half of the connector. This issue is still being addressed.

Changes were made to the HET front-end logic to correctly read out PHASIC counting rates and other changes. A revised CPU24 manual (Version 5) was issued accordingly.

Nineteen of the 20 H1 detector mounts had connectors attached and were shipped to Micron. Twenty-five of 40 H3 mounts were coupon tested and mechanically inspected, after which connectors were attached and the 25 mounts were shipped to Micron. There remain 15 H3 mounts to be completed. When received these had excess glue on them, so they were shipped back to the manufacturer to remove the glue.

The LET housing design has been significantly revised. Extra electrical shields and coaxial cables between the two LET PC boards were added to reduce cross-talk. These have made mechanical assembly more complex. To address this, the LET housing has been broken into more parts. Some of the LET mechanical parts have been made for the engineering boards.

Population of the SIT energy board (which we have had for ~ 2 months) is still awaiting final resolution of the SIT parts list.

SEPT parts were received and are awaiting painting/anodizing. The initial estimate for painting was excessive, so some parts will be anodized instead.

Considerable effort has gone into preparing for a full-up end-to end test at Caltech with all the SEP engineering units. Both HET and SIT have been shipped to Caltech and Larry Ryan (HET) and Peter Walpole (SIT) will go out to Caltech for the test. Much of this work involved developing the ability to send supplemented command messages with check sums and to upload on-board tables to SEP Central through the Caltech GSE (also with check sums). Commanding/uploading tables can be done through the internet from GSFC.

3.2.1. Next Month-

- Perform the end-to-end test of HET and SIT with the rest of SEP at Caltech.
- Complete processing of the last 15 H3 detector mounts and ship to Micron. This will complete all detector mounts for Micron.
- Complete an engineering version of the LET mechanical assembly and ship to Caltech.
- Complete painting/anodizing of the SEPT parts.
- Update ICD with APL to include mounting hole diameters and correct LET FOV.
- Update mass of SEP Main.
- Populate the HET flight boards and the SIT flight energy board.
- Work on defining the HET and SEPT radioactive sources to be supplied by GSFC.
- Get the detector life-test thermal vacuum system up and running with the prototype detectors.
- Close out remaining RFAs from CDR.

3.3. *Design Updates*

Need to update mass of SEP Main. This has been outstanding for awhile. Some progress has been made on this by weighing ETU boards.

3.4. *Outstanding Problems*

3.5. *New Problems*

Mostly slow schedule slipping.

3.6. *Top Risks*

No significant risks at GSFC? Need to ensure that manpower becomes available per the current plan.
We are running behind schedule with respect to detectors and the HET final electronics design. The HET delivery dates have been revised accordingly.

3.7. *Problem/Failure Quick Look*

4. Kiel/ESTEC (SEPT) Status

September 2003

4.1. *Summary of Status*

a) Canberra finally delivered 28 detectors (14 stacks) in week 39, causing delay of sensor integration.
b) Test of EM electronics revealed deficiencies in timing of coincidence/anticoincidence window. Remedy: changes in FPGA for flight models, will lead to 4 weeks delay.
c) Application of thermal coating is being done at GSFC, leading to delays which are in parallel to delays caused by late detector delivery (see 1.) and electronics redesign (see 2.).

4.2. *Major Accomplishments*

a) Canberra delivered 14 detector stacks, fully configured with RG178 cable, SSMC connectors and mounted in their flight housing. Incoming inspection and vacuum tests are ongoing for selection of total of 10 stacks (4 for FM, 4 for FM2, and 2 for flight spare).
b) SEPT Engineering model fully integrated, except for thermal hardware. Ready for SEP EM test at Caltech in October. Weight: 770 g without harness, bracket, and thermal hardware. Weight of SEPT-EM is representative for flight models as well.
c) 4 E-box housings for FM1 and FM2 sent to GSFC for application of black paint and Germanium black Kapton. 4 sensor housings will follow in October for application of black paint and Goddard Composite.
d) Budget meeting with German funding agency DLR to cover costs of environmental tests held on Sep. 30, without positive outcome. Efforts to get ESTEC to pay for tests are encouraging (vibration scheduled for 8/12-DEC-03, TV scheduled starting 15-DEC-03 for FM1 and 15-JAN-04 for FM2). Kiel will pay for acoustic test of EM, now scheduled for 10/11-NOV-03.
e) FM1-E and FM1-NS digital boards fully tested.
f) FM1-E and FM1-NS analog boards fully tested.
g) GSE power supply fully tested and calibrated. 4 GSE harnesses manufactured.
h) PDFE LAT test completed, final report pending.
i) Commercial part life test still ongoing (completion estimated for 10/10/03).
j) Modifications needed on the FPGA side to improve the (anti) coincidence performance. FPGA will be removed from FM1-E and FM1-NS digital boards and replaced. New delivery date to Kiel for FM1-E and FM1-NS is 27-OCT-03. FM2-E and FM2-NS deliveries to Kiel are foreseen for 19-NOV-03.

4.3. *Design Updates*

4.4. *Outstanding Problems*

1. Delay caused by late detector delivery, new FPGA, and thermal coating will lead to SEPT FM1 and FM2 delivery to Caltech in late January 2004.

4.5. *New Problems*

1. Magnets could not be shipped to GSFC for application of black paint (UPS and FEDEX refused shipment quoting “Dangerous Goods”). John Hawk proposed Chemglaze z306 which should be easier to apply. No distributor found in Germany yet.
2. Mass increased by 104 g (now 99 % measured, 1 % estimated).

4.6. *Top Risks*

4.7. *Problem/Failure Quick Look*

5. Caltech/JPL (SEP) Status

5.1. *Summary of Status*

Activities centered on detector development, electronics development, and flight and GSE software development.

Major Accomplishments:

- The LVPS ETU was delivered to Caltech.
- Micron Semiconductor completed the L3 detector order.
- The coupons for the flight Analog/Post-reg board passed inspection.
- Another good thermal vacuum run on a batch of detectors was completed.
- The LET EM board was tested, hay-wired, re-tested, and declared acceptable for flight. So no re-layout will be necessary.

Critical Milestones status:

- Milestone 13 (SEP-ETU LVPS Available) has been accomplished.
- Milestone 18 (HET-All Flight Detectors Received) has not been accomplished. Problems with the detector mounts have delayed progress.
- Milestone 19 (LET-All Flight Detectors Received) has not been accomplished. Mount problems also delayed progress although LET mounts are no longer an issue and good progress is being made.

Detectors:

- The second thermal-vacuum life test ended the first week in September. Of 3 membrane L1 detectors, 3 thick/thin L1 detectors, two prototype L2 detectors, and one L3 prototype detector, no failures occurred during the run. One other L3 detector was installed in the chamber but not run because it exhibited intermittent excess noise when it was first checked out. After the end of the run the problem with the noise L3 detector was investigated and appeared to be a problem with the setup rather than with the detector itself. This detector should be included in the third thermal-vacuum life test, which is planned to start in October.
- Micron Semiconductor delivered additional membrane L1 detectors. They report that of these, 9 are "grade A", meaning that they meet all of our specifications for flight detectors. The remaining 3 devices were designated as "grade B", indicating some minor deviation from the specification. We will test all of these detectors and determine whether any of the grade B devices are suitable for flight.
- Micron also completed their fabrication and testing of a quantity of H3 detectors. At the end of the month they reported that they had shipped the full complement of flight L3 detectors. These should arrive at Caltech the first week in October and be available for inclusion in the next thermal-vacuum life test.
- Micron now has received some H1 detector mounts and H3 mounts will be on their way to them in early October, so they should be assembling and testing HET detectors, as well as LET L2 and additional L1 detectors, in the next month.
- A meeting was held on September 26 with personnel from Micron Semiconductor (who stopped on their way to visit another customer), and STEREO detector status was reviewed.

Electronics:

- Most work was focused on the LET FE/logic board. All layout problems were found and fixed via haywires, such that low threshold operation was achieved with all 54 pulse-height analyzers simultaneously. After discussion with QA and fabrication experts at JPL we decided that the LET FE/logic board layout was adequate for the flight build without any re-layout.
- LET firmware consists of routines that interface with the hardware (being written by Rick Cook) and event processing, sorting and formatting routines (being written by Andy Davis). Significant progress was made on the former and the PHASICs and other hardware on the LET board has been checked. A main task remaining in the hardware interface/control category is to write and test the leakage current balancing algorithm.
- The interface between the Rick Cook and Andy Davis software has been partially defined. The flow chart and requirements for the Andy Davis S/W have been refined to account for hardware realities (such as FE cross-talk and "hazard" events). Some iteration is still needed to finalize the design of the on-board event prioritization and sorting scheme.
- Some minor modifications were made to the LET MISC Actel design to rearrange the order of bits in the event data to speed event sorting in the MISC S/W. Otherwise the MISC Actel design has been stable and working well.
- The LET and SEP Central engineering boards and S/W will be ready to support the SEP suite EM integration planned for the second week in October.
- I/F test between EM LVPS and EM SEP_Central electronics carried out successfully. EM LET was also included in the test, while the rest of SEP sensor loads were simulated.
- SEP_Central Analog/Post-Reg flight boards received from Cirtech; test coupons passed the inspection and the fabrication is scheduled to start in early October when calibration of solder station is complete.
- SEP_Central Logic flight boards received from Pioneer Circuits; test coupon inspection is under way at GSFC.
- Flight parts kitting mostly done for HET, SEP_Central Logic and Analog/Post-Reg boards. The heritage parts are expected back from up-screening in early October.
- PHASIC hybrid burn-in started on 6 more hybrids. The previous 4 flight parts have passed through lead-forming and final screening.
- Soldering re-certification Part II completed at JPL for the flight assembly operator. The action item list from QA inspection is being worked on.
- TQCM from GSFC received; Kelly Henderson visited us twice since the CC workshop, gave us tutorial on TQCM use, and installed NVR witness plates in the clean rooms and detector test T/V chamber.
- Implemented all of Parts Control Board recommendations and continued work on SEP thermal hardware common buy.

Software (Davis):

- Worked on LET flight software and PHASIC temperature testing software.

GSE:

- Modified software to locate LET Science Frames (one minute of LET Science data) in the telemetry packets to be consistent with the most current LET Science Frame format. LET Science Frames are now variable length and span multiple CCSDS packets. The algorithm that locates the LET Science frame now requires all the packets for one LET Science Frame to have the same UT, valid packet checksums, a valid set of ApIds, to be self-consistent in length, and have a valid frame checksum. Any LET Science packets that fail to meet these criteria will be sent to the unprocessed packet file for further analysis and corrective action. This software is currently waiting for testing with the SEP/LET flight software.
- Started developing software for displaying scatter plots of LET events. Have completed the software that manages the actual display of the data points and user interactions with the display, i.e. scale changes, resizing, etc. The software that selects events and generates data points from the raw LET events has not been started.
- Corrected minor problems with the time history plots of SEP/LET data. In the previous version, there were problems in changing from a linear to a log scale and other details in the display. These problems are now solved.

5.2. *Design Updates*

- Resource updates will be sent separately.

5.3. *Outstanding Problems*

- The problems with the two flight Actels are still being investigated by Actel.
- All detector mount problems appear to have been resolved.

5.4. *New Problems*

- No new problems this month.

5.5. *Top Risks.*

- The budget is very tight with no reserve being held at Caltech.

5.6. *Problem/Failure Quick Look*

- None.

5.7. *Lien List*

- Budget does not contain funding for investigations of part failures or contamination failures, re-makes of boards if coupons fail, etc. The amounts and timing of these types of expenditures are largely unknown. Board re-makes are in the $6,000 to $12,000 range, per board type. There are four board types. The budget does contain funding for board reworks, including adding haywires, etc.
- Unfunded schedule reserve: ~$25,000 (if we deliver in September 2004 as required rather than July 2004 as currently planned).
- Possible under-budgeting of environmental testing and bakeout. $100K has been allocated. However, recent estimates suggest that the thermal balance/thermal vacuum test may require about 3 weeks. Recent cost estimates at JPL suggest that that might take the entire $100K. We are investigating other places for the environmental test program where the costs may be less.

6. SIT MONTHLY TECHNICAL PROGRESS REPORT

September 2003

6.1. *SUMMARY of STATUS*

a. SIT TELESCOPE - Prototype is in house and working. Flight solid state detectors are in house, awaiting test. Flight Microchannel plates are in house and are tested. Foils are at GSFC.
b. SIT TOF System - FM1 has been downgraded to ETU and returned to UMd. Work is proceeding at MPAe to generate a new FM1 and FM2.
c. SIT Energy/Logic System – ETU Energy system, ETU TOF system and the ETU motherboard have been integrated with the ETU Logic system including front-end logic and MISC. Testing is underway at Umd.
d. SIT HVPS - Flight HVPS ETU is being built at UCB.

6.1.1. Schedule Changes

The current SIT schedule is available from Jim Rogers

6.2. *MAJOR ACCOMPLISHMENTS*

6.2.1. This Month

- TOF: The DTOF parts list was approved and work on the flight unit was restarted.
- ETU: A new ETU logic board and mother board were laid out and the boards fabricated.
- Energy board: Parts were ordered and FETs were submitted to Ron Jackson at UCB for DPA to comply with parts review board requirements for the energy board components.
- Detectors: SSDs were delivered to GSFC for testing.
- ESD: Walpole took and passed the ESD awareness course.
- Cleanliness: The clean bench area to be used for flight component testing was certified.

6.2.2. Next Month

Next month we will complete the ETU, take it to Caltech for a SEP ETU integration. We will install a new ETU Actel which has been modified to meet the new flight memory timing requirements. We will continue flight software development and testing with GSFC.

6.3. *DESIGN UPDATES*

6.3.1. Resources

	Last Month	This Month	Change
Mass (kg) *	1.46	1.46	0
Power (W)	1.56	1.56	0.0
Telemetry (bps)	418	418	0

* Includes 200g book-kept by GSFC for SIT structure
A new estimate of Actel power for the flight units indicates that power will increase. Previous estimates had neglected the effect of the triple gates in the flight units for single-event upset protection.

6.4. *OUTSTANDING PROBLEMS*

We are continuing to work Energy parts issues.

6.5. *NEW PROBLEMS*

6.6. *NEW RISKS*

6.7. *PROBLEM/FAILURE QUICK LOOK*

Starts at first turn-on of flight hardware.

ID #	Description	Assignee	Opened	Closed

7. CESR (SWEA) Status

CESR- TOULOUSE- France **Author : Claude Aoustin / Project Manager**

SWEA PROGRESS REPORT # 24
(October 10, 2003)

September 2003

CESR is in charge of :
- Electrostatic analyzer with deflectors, grids and Retractable Cover
- Detector consisting of two MCP rings
- Amplifiers and discriminators
- 3 High voltages

7.1. *Summary of Status*

7.1.1. ETU1

Delivery to UCB was planned for 12/07/2002 : done 26/09/2002

7.1.2. ETU2

Mechanical fabrication 100 % done
Integration done for the vacuum test configuration.
Electronic boards tested (100 %).

7.1.3. FM1 / FM2

Mechanical fabrication 100 % done.
Grids for FM1 delivered on July 31 , FM2 delivered on September 12.
Surface treatment of the analyzer spheres done.
Surface treatment (gold, alodine) done.
Pin Puller integrated and tested.
Electronics boards fabrication :

- Done for HV coupling board
- Done for amplifiers board
- Done for the HV board

7.2. *Major accomplishments*

FM1 :

- Final integration of FM1 done July 31.
- MCP characterization was done before the final integration without external sphere and grids.
- Experiment fully integrated in vacuum.
- Calibration setting in place. Automatic rotation system checked with new software.
- Calibration done for all of the polar and azimuth angles at 1keV.

FM2 :

- Ampli board tested, HV board tested.
- Thermal test on the HV board done :
- HM 402 P 10 from VMI failed at -70°C. Has been replaced and tested again successfully.

7.3. *Design Updates*

Mass : 967 g (EM is 950g without cover opening mechanism)
Power : 446 mW min ; 662 mW max

7.4. *Outstanding Problems*

Telecon about SWEA parts list took place on September 26.
HV resistors need life test 1000 h. under preparation.

7.5. *New problems*

HV multiplier from VMI HM 402 P 10 failed at -70°C !

7.6. *Top Risks*

7.7. *Problem Failure Quick Look*

See section 7.5. PFR pending.

8. GSFC (MAG) Status

- ETU#2 interface tests at UCB passed (end-to-end test from sensor to POC). Some EMC tests still to perform.
- FM PWBs have been manufactured and are ready to load as soon as coupons are checked.
- FM card trays have been provided to GSFC by UCB

9. EPO at UCB

Monthly E/PO Report September, 2003

Formal Education:

We have made corrections to the IMPACT boom lesson and resubmitted it to NASA's Sun Earth Connection Education Forum to get further feedback. The Magnetism lesson was put on the web for teachers and the public to access.

We further prepared for the workshop about the Sun at the Society for the Advancement of Chicanos and Native Americans in Science (SACNAS) National Conference in early October.

Informal Education and Public Outreach:

We started a web page to explain the design, testing, and building of the IMPACT boom.

The sounds project has again begun. We have begun discussions with Edmund Campion at the Center for New Music and Audio Technologies at UCB.

Cross Cutting:

A proposal was written to the NASA STEREO E/PO personnel at Goddard to fund the IMPACT E/PO for FY04, FY05 and L+30D activities.

An AGU abstract was submitted for a paper that presents the Teacher's Magnetism Guide in terms of the philosophy of Backward Design.

Respectfully Submitted,
IMPACT E/PO scientists Nahide Craig, Laura Peticolas