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Subject: IMPACT Monthly Technical Progress Report, Contract NAS5-00133

Lil:

Enclosed is the monthly technical progress report for the STEREO IMPACT project for the month of August 2003.

Sincerely,

David Curtis
IMPACT Project Manager
University of California, Berkeley

CC:

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IMPACT Team

1. IMPACT Overview

This report is presented in sections by institution. Section 1 is an IMPACT Project Manager / System Engineer's overview.

1.1. *Contracting / Funding*

Funding through the end of FY03 is in place. Because of pipe-line delays in the system through to the subcontractors (Caltech and UMd) it is important that IMPACT be funded somewhat in advance of expected spending.

An updated budget based on the latest schedule planning and costing estimates has been submitted. No additional FY03$ are required. This new budget was presented and discussed at a meeting with Project.

1.1.1. Liens

This is a list of Lien. Liens for activities at other institutions are sometimes repeated in their subsections of this report. These liens are estimated additional costs that might be incurred if problems happen. Only problems with a significant likelihood of occurrence are tracked. These liens are usually associated with risks in the risk list (see section 1.5), and you can see the predicted likelihood of occurrence there.

UCB:

No.	Cause	Amount	Date
1	LVPS schedule delays extend manpower (Risk UCB29). Cost a 1-month delay at full LVPS team spending rate.	$35,000	01/04
2	Late failure in thermal vac requires rework/retest (Risk UCB27, etc).	$30,000	02/04
3	Testing failure requires rebuild/retest a board (using existing spare parts)	$20,000	~02/04
4	EMC rework and retest required (Risk UCB11). Assume rework can be done in a week or two.	$30,000	05/04
5	Schedule delays cause the consumption of boom suite schedule contingency (various risks). Cost 35 days of contingency at UCB I&T team rate.	$50,000	07/04

Caltech:

No.	Cause	Amount	Date
1	Budget does not contain funding for investigations of part failures or contamination failures, re-makes of boards if coupons fail, etc. The amounts and timing of these types of expenditures are largely unknown. Board re-makes are in the $6,000 to $12,000 range, per board type. The budget does contain funding for board reworks, including adding haywires, etc.	$12,000	12/03
2	Unfunded schedule reserve (if we deliver in September 2004 as required rather than July 2004 as currently planned).	$25,000	8/04
3	Bakeout plans need to be firmed up. May result in more time in JPL bakeout chambers	$20,000	7/04

UMd:

No.	Cause	Amount	Date
1	SIT foils fail acoustic test	$20,000	2/04
2	SIT Vibration (currently planned to be combined with HET instruments, but may not work out)	$15,000	2/04
3	Parts screening (some parts not yet Oked by PCB and may need addition screening)	$10,000	9/03
4	Particle Calibration at BNL. This is desired but not required.	$20,000	11/03
5			
6			

GSFC (Tycho):

No.	Cause	Amount	Date
1			
2			
3			
4			
5			
6			

1.2. *Significant System-Level Accomplishments*

- Participated in Contamination Control Committee telecon
- Contamination Control Workshops presented at Caltech and UCB
- Held a number of Parts Control Board meetings to review and approve parts lists for boards ready for flight build

1.3. *System Design Updates*

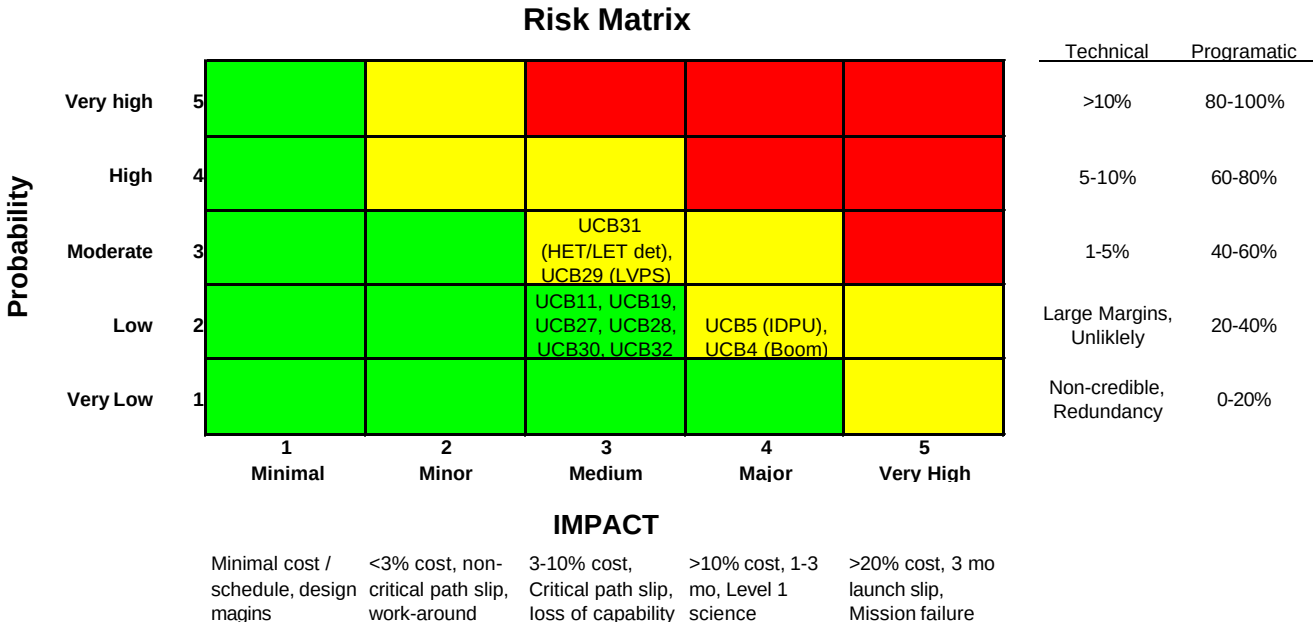
- None

1.4. *System Outstanding Issues*

- New boom cork contamination waiver submitted, test results submitted for review.

1.5. *Top 10 Risks*

Top 10 risks are attached. No significant new risks added; some risk levels have changed due to mitigations, causing some rearrangement, and some risks have been restated due to changing circumstances.


Risk Matrix
Probability
Very high 5
High 4
Moderate 3
Low 2
Very Low 1
UCB31 (HET/LET det), UCB29 (LVPS)
UCB11, UCB19, UCB27, UCB28, UCB30, UCB32
UCB5 (IDPU), UCB4 (Boom)
1 Minimal
2 Minor
3 Medium
4 Major
5 Very High
IMPACT
Technical
Programatic
>10%
80-100%
5-10%
60-80%
1-5%
40-60%
Large Margins, Unliklely
20-40%
Non-credible, Redundancy
0-20%
Minimal cost / schedule, design magins
<3% cost, non-critical path slip, work-around
3-10% cost, Critical path slip, loss of capability
>10% cost, 1-3 mo, Level 1 science
>20% cost, 3 mo launch slip, Mission failure

IMPACT Top Ten Risks 8/2003

No.	Risk Item	Score	Mitigation	Mitigation Schedule						
				PDR	EM Test	CDR	Sub-system Test	System Test	Env test	Early Orbit Test
UCB_5	IMPACT boom is a new design. Failure could affect Imager pointing requirements as well as boom-mounted instruments.	MEDIUM	Design for reliability. Early prototype testing. Qual model testing completed. Adequate force margins demonstrated.	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	LOW
UCB_4	The IDPU is a single point failure mechanisim for the IMPACT suite and PLASTIC	MEDIUM	IDPU is a simple, reliable system. Extra attention has been paid to ensuring its reliability, minimizing the risk of fault propagation. Extensive EM & FM testing	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM
UCB_31	HET/LET ETU detector mounting difficulties impacting schedule	MEDIUM	Idnetify and solve problems; bring in outside experts to evaluate process, continue with flight detector fab in parallel	MEDIUM	MEDIUM	MEDIUM	MEDIUM	LOW	LOW	LOW
UCB_29	LVPS behind schedule, on critical path; further slipping could delay delivery to spacecraft	MEDIUM	Add manpower to LVPS task to avoid further slippage	MEDIUM	MEDIUM	MEDIUM	MEDIUM	LOW	LOW	LOW
UCB_11	Stringent EMI requirements may delay schedule if testing fails	LOW	Careful design, ETU power converter testing, early system testing	MEDIUM	MEDIUM	MEDIUM	LOW	LOW	LOW	LOW
UCB_27	Actel timing differences between flight & ETU parts may cause failures late in testing impacting delivery schedule	LOW	Do FM Thermal Vac early to allow time for finding and fixing timing problems; for designs on the critical path, consider installing a flight Actel in the ETU & thermal cycle.	MEDIUM	MEDIUM	MEDIUM	LOW	LOW	LOW	LOW
UCB_28	Thermal limitations of detectors result in a low bakeout temperature which might require a very long bakeout impacting delivery schedule	LOW	Bakeout subsystems prior to detector integration to reduce time of instrument-level bakeout; early bakeout	MEDIUM	MEDIUM	MEDIUM	LOW	LOW	LOW	LOW
UCB_19	Concern about fragility of ITO surfaces required to meet ESC requirements; failure will impact SWEA science	LOW	Replace ITO with more robust solution where possible; test ITO surfaces during I&T and replace when required	MEDIUM	MEDIUM	MEDIUM	LOW	LOW	LOW	LOW
UCB_32	Parts Review Boards & Parts Waiver process could delay flight fabrication	LOW	Work to get parts lists approved, waivers into system where PCB cannot agree.	MEDIUM	MEDIUM	LOW	LOW	LOW	LOW	LOW
UCB_30	SECCHI magnetics (especially filter wheen motor) may exceed magnetics requirement, impacting MAG science	LOW	Testing completed, shielding implemented.	MEDIUM	MEDIUM	MEDIUM	MEDIUM	LOW	LOW	LOW

2. Berkeley Status

2.1. *Summary of Status*

Schedule status through June has been provided separately.

2.2. *Major Accomplishments*

SWEA/STE:

- Continued to performed vacuum calibration tests on the combined SWEA/STE ETU stack
- SWEA/STE flight boards re-layed out and in review.
- STE flight detector boards in fabrication.
- STE, SWEA Pedestal, and STE-U preamp housing in flight fab

IDPU:

- First flight unit DCB completed and tested. Second unit in fabrication. Build cannot complete until ROM programmed and installed, which is pending final PROM software acceptance tests and ETU spacecraft interface test.
- Flight Software: Working on PROM software acceptance test, Working on Build 3 for IMPACT.
- PLASTIC software Build #2.3 in progress, with a target delivery date of September for the IDPU/PLASTIC ETU interface test.

LVPS/HVPS:

- SIT HVPS FM #1 in final tests for delivery in September
- SWEA/STE LVPS in re-layout for flight
- PLASTIC LVPS ETU In test at UNH, re-layout for Flight in progress.
- SEP LVPS ETU build complete (including power sequencing for Actel current spike problem), testing in progress, expect delivery to Caltech for integrated ETU test mid September.
- Working to add power sequencing to IDPU LVPS

Boom:

- Qual Boom thermal vacuum test complete which completes the qualification cycle.
- A deployment failure during thermal vac is the result of a PFR. Problem was diagnosed, fixed, and re-tested.
- Preparations for Thermal Balance test on Qual boom in progress for a test in September.
- Flight build activities have started. Drawings are being updated for flight parts and the flight tube order has been released. The first batch of flight tubes was received and rejected. Have met with the manufacturer to resolve problems.

GSE:

- Continued additions to C&T GSE, SWEA/STE GSE.

2.3. *Design Updates*

- None.

2.4. *Outstanding Problems*

2.5. *New Problems*

2.6. *Top Risks.*

- LVPS schedule tight

2.7. *Problem/Failure Quick Look*

ID #	Description	Assignee	Opened	Closed
1001	Qual boom deployment failure in Thermal Vac	McCauley	2003-08-15	

3. GSFC (SEP) Status

STEREO/IMPACT/SEP/GSFC Progress Report for August, 2003 – (von Rosenvinge, Baker, Hawk, Reames, Shuman, Wortman)

3.1. *Summary of Status*

The delivery dates of the HET flight units have been revised from 12/23/03 and 1/22/04 to 2/28/04 and 3/15/04. The new delivery dates are needed for various reasons: (1) problems with obtaining fully qualified detector mounts has slowed delivery of flight detectors, (2) additional time was needed to complete evaluation of the engineering electronics, (3) approval of the flight parts list has been slow, and (4) flight PHASICs will be delivered later than previously expected.

3.2. *Major Accomplishments*

A revised budget was submitted to the STEREO Project Office.

The HET flight PC board layout was updated from the engineering test unit layout and submitted for fabrication. The HET flight boards should be received in mid-September. All parts for the HET flight boards have been approved. However questions have been raised relative to the detector connectors and how many mate/demates they can tolerate. A mate/demate test is currently underway. We expect this test to have a positive outcome.

The remaining 24 L1 detector mounts and the remaining 11 L2 detector mounts were shipped to Micron. Nineteen of the 20 H1 detector mounts have been received and have had excess glue removed. In addition, the coupon tests and the mechanical inspection have been completed for these mounts so that we are now ready to mount connectors on these mounts. Twenty-five of 40 H3 mounts have finally been received and coupon testing and mechanical inspection are beginning. There remain 15 H3 mounts to be remade.

A Low Voltage Power Supply box is in fabrication and will be shipped to UCBerkeley shortly. The LET housing design has been revised. One revision was to break the housing into more parts, which will make final assembly easier.

Population of the SIT energy board (which we have had for ~ 1 month) is still awaiting final resolution of the SIT parts list.

Thermal models were delivered to APL.

3.2.1. Next Month-

Process new H1 and H3 detector mounts and ship to Micron.
Update ICD with APL to include mounting hole diameters and correct LET FOV.
Update mass of SEP Main.
Complete verification of the revised HET Actel design (specifically the front-end logic) and burn a flight version.

Populate the HET flight boards.
Work on defining the HET and SEPT radioactive sources to be supplied by GSFC.
Get the detector life-test thermal vacuum system up and running with the prototype detectors.

3.3. *Design Updates*

Need to update mass of SEP Main. This has been outstanding for awhile. Some progress has been made on this by weighing ETU boards.

3.4. *Outstanding Problems*

3.5. *New Problems*

Mostly slow schedule slipping.

3.6. *Top Risks*

No significant risks at GSFC? Need to ensure that manpower becomes available per the current plan.
We are running behind schedule with respect to detectors and the HET final electronics design. The HET delivery dates have been revised accordingly.

3.7. *Problem/Failure Quick Look*

4. Kiel/ESTEC (SEPT) Status

August 2003

4.1. *Summary of Status*

a) Detector delivery from Canberra delayed by one more week, now expected in week 38.
b) Electronics manufacturing and test according to plan. No further delays unless test of the analog boards reveal unexpected problems.

4.2. *Major Accomplishments*

a) Alodine 1200 surface treatment of all aluminium parts for flight units finished (not yet for flight spare).
b) ETU magnetic deflection test passed (using Bi207 conversion electrons).
c) ETU mechanical function test passed (activating pinpuller on nominal and redundant circuit). Decision taken to use only nominal circuit for flight units, as APL does not provide additional command service for redundant circuit. Wire redundancy will be provided up to SEPTNS-J3 and SEPTE-J3.
d) Progress on purge tube fittings: SEPT will use barb, .125 OD, .063 ID tube.
e) Progress on coax cable RG178 and magnetic cleanliness: Mario Acuna tested and approved sample of RG178 which will be used both for sensor and inside E-box.
f) Reached agreement with Sandy Shuman on thermal coating for SEPT: owing to sophisticated application procedures and ITAR issues, all parts will be sent to GSFC for coating, even the magnets. Risk for further delays.
g) Reached agreement for installation of remaining thermal hardware (thermostats, op-, non-op-heater, MLI): at GSFC in January 2004 prior to SEPT delivery to Caltech for I & T.
h) FM1 And FM2 analog board completed.
i) FM2 digital board tested successfully.
j) GSE power supply model 2 delivered and being tested. All modes implemented on the GSE.
k) One new harness manufactured, a second in progress.
l) PDFE LAT tests started.
m) Life test of ADG704, ADG713 and TLC2262 started.

4.3. *Design Updates*

4.4. *Outstanding Problems*

1. Delay in detector delivery (see above).
2. Budget problem for environmental tests. The German funding agency (DLR) is informed. ESTEC (Trevor Sanderson) is informed, working on a solution.

4.5. *New Problems*

4.6. *Top Risks*

4.7. *Problem/Failure Quick Look*

5. Caltech/JPL (SEP) Status

5.1. *Summary of Status*

Activities centered on detector development, electronics development, and flight and GSE software development.

5.1.1. Major Accomplishments:

- For the first time all 4 EM boards for which Caltech is responsible were available and working together: SEP Central Logic, Analog/Post-reg, Bias Supply, and LET (with an L1 detector installed and stimulated with alpha particles).
- Analog/Post-reg and SEP Central Logic board designs submitted to vendors for flight fabrication, the first flight boards from SEP to go in.
- Two thermal vacuum runs on LET detectors have produced only one possible detector failure (and that failure might be in the lab electronics rather than the detector).
- A Contamination Control Training class was held at Caltech during August.

5.1.2. Critical Milestones status:

- Milestone 13 (SEP-ETU LVPS Available) has yet to be accomplished. We have not been losing schedule time due to this late delivery as we are using bench supplies to substitute for the LVPS.
- There were no milestones in August for LET or SEP Central on the IMPACT Critical Milestones chart dated 7/31/03.

Detectors:

- The second thermal-vacuum life test run is nearly completed (should end on September 4). This run included six L1 detectors (3 of the membrane devices and 3 of the thick/thin version), two L2 prototype detectors (installed in their mounts incorrectly, but otherwise good), and two L3 prototype detectors. With the exception of one L3, all detectors performed well. The problem L3 detector exhibited intermittent periods of elevated noise. When the run is completed we will investigate whether this noise is related to the detector or to the test setup (previously, during alpha-particle testing, these noise increases were not observed).
- Micron performed vibration and thermal cycling tests of 12 L1 detectors (all membrane-type). Preliminary indications are that 9 of these should meet the flight L1 specifications. Micron expects to ship completed L1 detectors to Caltech the first week in September, after they complete a 168-hour test operating under bias.

Electronics:

- Check out of the LET front-end and MISC rigid-flex board continues. The board worked well enough to support the test of all four installed PHA hybrids. All of LET PHAs were operated separately at the intended thresholds and dynamic range settings. A problem with this low threshold operation was found only for one of the L2 detector segments and this is due to a layout problem that caused coupling from a digital control signal to that L1 detector preamp input.

- A single L1 detector was connected and operated with the EM bias supply. The performance of the attached PHAs (three segments) was as expected except for some retriggering discussed below, with no noticeable systematic noise present. Tests with a full complement of detectors are planned for the coming weeks.
- The L1 detector was stimulated with alpha particles. We noticed that thresholds for two of the three detector segments had to be raised slightly to prevent retriggering following the alpha particle pulses. The same retriggering behavior was produced with pulses from the built-in test pulsers and it was found to occur only over a limited range of test pulse amplitudes. Further investigation suggests that the problem is unlikely to be related to PCB layout, but is rather in the VLSI design (and therefore is something we will have to live with). Further assessment of this problem is underway, including SPICE simulations.
- An intermittent problem was observed with the LET MISC. The FORTH system could always be booted successfully from the SEP MISC EEPROM but the downloading of software through SEP did not always work and often crashed LET. Investigation determined that the software transfer through SEP to LET was not the problem; rather the problem occurred in LET when correctly transferred source code was being compiled into the FORTH dictionary. The exact failure mode was not entirely reproducible. However on several occasions corruption of RAM contents were noted following attempted compilations. While no specific failure mechanism was uniquely identified, it appeared that RAM access timing was marginal. We had received a memo from the RAM manufacturer alerting us to the need to hold the address lines stable for at least 5 nsec prior to the release of the RAM chip enable signal at the end of a RAM access cycle. We altered the MISC Actel design to ensure this spec and found that with the new design installed the LET MISC no longer had the compilation problem. While it is likely that fixing the RAM access timing marginality fixed the compilation problem, it is also possible that some other aspect of the design is marginal. So we will soon begin temperature and voltage margin testing. The MISC design change will be incorporated into the SEP Central MISC and be relayed to GSFC for consideration for SIT and HET.
- I/F test between LET ETU and SEP Central electronics was successful. Bias Supply was tested with L1 detector only; soon to follow with L2/L3.
- Both the EM Analog/Post-reg and the EM Bias Supply board passed temperature testing over the range –40C to +55C.
- SEP Central Analog/Post-Reg flight board submitted for fabrication to Cirtech with 2-week delivery.
- SEP Central Logic flight board submitted for fabrication to Pioneer Circuits with 2-week delivery.
- Flight parts kitting started for HET and SEP Central Logic boards. The heritage parts were sent for up-screening to local vendor, Tandex Test Labs.
- PHASIC hybrid burn-in boards assembled and burn-in started on 4 hybrids.
- Soldering re-certification Part I completed at JPL for the flight assembly operator. QA inspection of flight-like workmanship on EM Logic board performed and action item list will be addressed shortly to rectify the problem areas.
- Contamination control workshop attended and areas of concern discussed to some degree; the remaining items will be addressed with the new local Contamination Control Engineer, Kelly Henderson.

Software:

- Worked on LET onboard event processing software.

GSE:

- Worked on GSE software and compiled a list of questions that need answering by the LET team before the LET software can be finalized:
    - Has the proposed Andrew Davis LET event header format been accepted?
    - What about the Andrew Davis SYNC pattern proposal?
    - Define the 24-bit stim event block.
    - Define locations of 1-minute live-time monitor stim event counters.
    - Need paragraph giving definitions of the 8 live time related counters.
    - Define 16-bit compression algorithms used with 1-minute counters.
    - Will there be a need for 12-bit compression of any 1-minute counter?
    - Will all packets for a LET Science Frame have the same UT?
    - Any new additions to the Science Frame format?

5.2. *Design Updates*

- Resource updates will be sent separately.

5.3. *Outstanding Problems*

- The problems with the two flight Actels are still being investigated by Actel.
- All detector mount problems appear to have been resolved.

5.4. *New Problems*

- 2 of 7 PHASICs failed PIND testing. The cause is thought to be known and corrective actions will be taken on the next batch of 10. The 2 failed units will be set aside and repaired later if necessary.
- A retriggering problem was discovered in the VLSI (part of the PHASICs). This problem will be dealt with by raising the thresholds slightly. The VLSI will not have to be rebuilt.
- The LET MISC exhibited an intermittent compilation problem that is likely due to marginal RAM access timing. The timing was fixed and the problem went away. Further tests, voltage margin and temperature, are planned to see if there are any other marginal timing issues.

5.5. *Top Risks.*

- The budget is very tight with no reserve being held at Caltech.

5.6. *Problem/Failure Quick Look*

- None.

5.7. *Lien List*

- Budget does not contain funding for investigations of part failures or contamination failures, re-makes of boards if coupons fail, etc. The amounts and timing of these types of expenditures are largely unknown. Board re-makes are in the $6,000 to $12,000 range, per board type. The budget does contain funding for board reworks, including adding haywires, etc.

- Unfunded schedule reserve: ~$25,000 (if we deliver in September 2004 as required rather than July 2004 as currently planned).

6. SIT MONTHLY TECHNICAL PROGRESS REPORT

6.1. *SUMMARY of STATUS*

a. SIT TELESCOPE - Prototype is in house and working. Flight solid state detectors are in house, awaiting test. Flight Microchannel plates are in house and are tested. Foils are at GSFC.
b. SIT TOF System - FM1 has been downgraded to ETU and returned to UMd. Work is proceeding at MPAe to generate a new FM1 and FM2.
c. SIT Energy/Logic System – ETU Energy system, ETU TOF system and the ETU motherboard have been integrated with the ETU Logic system including front-end logic and MISC. Testing is underway at Umd.
d. SIT HVPS - Flight HVPS ETU is being built at UCB.

6.1.1. Schedule Changes

The current SIT schedule is available from Jim Rogers

6.2. *MAJOR ACCOMPLISHMENTS*

6.2.1. This Month

TOF: The ATOF parts list was approved and work on the flight unit was restarted.

ETU: ETU testing was successfully completed at Caltech. Caltech however reported a number of problems relating to assembly issues on the ETU logic board which had to be fixed at Caltech before testing could be completed. When returned to us, this board was reworked by technicians at the Umd physics department shop, and a number of inadequate solder joints were discovered and repaired. We have decided to have all further ETU soldering done at the shop rather than within the Space Physics group to prevent a recurrence of this problem.

Software: The flight software was troubleshot and corrected so that we now get PHA events and rates read out in their proper packets. GSE software was also written at Umd to display and characterize pulse height events and rates. A number of small items have been identified that need fixing – a missing rate, a missing event count in the PHA packets, and missing rate compression – but these will be addressed next month.

Detectors: MCP test data were reviewed and an assignment was made of which plates would be flown in which position in the telescopes.

ESD: An informal ESD review was held at Umd and the recommended equipment was ordered.

6.2.2. Next Month

Next month we will complete the flight design of the logic board, lay it out and build a new ETU. We will also re-layout the motherboard to fix existing problems. We still hope to resolve the parts issues on the DTOF system to allow MPAe to finally begin construction of the flight TOF boards and the parts issues on the Energy board so that assembly can be performed at GSFC.

6.3. *DESIGN UPDATES*

6.3.1. Resources

	Last Month	This Month	Change
Mass (kg) *	1.46	1.46	0
Power (W)	1.56	1.56	0.0
Telemetry (bps)	418	418	0

* Includes 200g book-kept by GSFC for SIT structure
A new estimate of Actel power for the flight units indicates that power will increase. Previous estimates had neglected the effect of the triple gates in the flight units for single-event upset protection.

6.4. *OUTSTANDING PROBLEMS*

We are continuing to work TOF parts issues.

6.5. *NEW PROBLEMS*

We are working Energy parts issues.

6.6. *NEW RISKS*

6.7. *PROBLEM/FAILURE QUICK LOOK*

Starts at first turn-on of flight hardware.

ID #	Description	Assignee	Opened	Closed

7. CESR (SWEA) Status

CESR- TOULOUSE- France **Author : Claude Aoustin / Project Manager**

SWEA PROGRESS REPORT # 23
(September 14, 2003)

August 2003

CESR is in charge of :

- Electrostatic analyzer with deflectors, grids and Retractable Cover
- Detector consisting of two MCP rings
- Amplifiers and discriminators
- 3 High voltages

7.1. *Summary of Status*

7.1.1. ETU1

Delivery to UCB was planned for 12/07/2002 : done 26/09/2002

7.1.2. ETU2

- Mechanical fabrication 100 % done
- Integration done for the vacuum test configuration.
- Electronic boards tested (100 %).

7.1.3. FM1 / FM2

- Mechanical fabrication 100 % done.
- Grids for FM1 delivered on July 31 , FM2 delivered on September 12.
- Surface treatment of the analyzer spheres done.
- Surface treatment (gold, alodine) done.
- Pin Puller integrated and tested.
- Electronics boards fabrication:
  - Done for HV coupling board
  - Done for amplifiers board
  - Done for the HV board

7.2. *Major accomplishments*

- Mechanical fabrication of the grids done on FM1.
- Final integration of FM1 done July 31.
- MCP characterization was done before the final integration without external sphere and grids.
- Experiment fully integrated in vacuum.
- Calibration setting installation. New automatic rotation system checked with new software.
- Ready to start the calibration.

7.3. *Design Updates*

Mass : 1040 g (EM is 950g without cover opening mechanism)
Power : 446 mW min ; 662 mW max

7.4. *Outstanding Problems*

Telecon about SWEA parts list took place on August 22.
More details to be added about quality levels for Resistors, Diodes and Capacitors. Under preparation.
Answer to comments on materials list sent. Samples of EP851 and Delrin sent to Johanne Uber.

7.5. *New problems*

None

7.6. *Top Risks*

7.7. *Problem Failure Quick Look*

None

8. GSFC (MAG) Status

ETU#2 MAG testing in complete. ETU#2 on its way to UCB for interface tests
FM board layout modifications in progress, to be fabricated next month.
Flight parts procurement and screening to be complete.

9. EPO at UCB

Monthly E/PO Report August, 2003

Formal Education:

We received feedback from NASA's Sun Earth Connection Education Forum regarding the IMPACT boom lesson and began to make corrections from their input.

We prepared for the SACNAS national conference. In early October at this conference, we will teach classroom activities about the Sun, and will give a lecture about the sun and the STEREO mission at a teacher professional development workshop.

Public Outreach:

Several more copies of the boom movies made in July were put on CDs for STEREO personnel. A high school student helped to shorten the movie of the vacuum chamber assembly in order to place it on the STEREO E/PO web page.

STEREO Mission:

The movies of the boom testing were sent to Rachel Weintraub at the Goddard Visualization Center so that they might be included in the STEREO pre-launch visualization project. L. Peticolas continued to discuss via email with the group at Goddard regarding this project to ensure that IMPACT is represented.

Respectfully Submitted,
IMPACT E/PO scientists Nahide Craig, Laura Peticolas