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Subject: IMPACT Monthly Technical Progress Report, Contract NAS5-00133

Lil:

Enclosed is the monthly technical progress report for the STEREO IMPACT project for the month of June 2003.

Sincerely,

David Curtis
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IMPACT Team

1. IMPACT Overview

This report is presented in sections by institution. Section 1 is an IMPACT Project Manager / System Engineer's overview.

1.1. *Contracting / Funding*

Funding through the end of FY03 is in place. Because of pipe-line delays in the system through to the subcontractors (Caltech and UMd) it is important that IMPACT be funded somewhat in advance of expected spending. There is some concern over the pending financial services shutdown at GSFC, particularly for the GSFC team members. Even with the best planning there will be unexpected needs during this interval that could threaten our schedule.

A new budget plan for IMPACT has been agreed upon that fits within the funding constraints without sacrificing hardware. Some pre-launch science support has been cut, but development of level 1 data reduction software has been maintained. An official version of this budget has been submitted through channels at Berkeley for a contract mod.

1.2. *Significant System-Level Accomplishments*

- Held Protoflight boom status meeting (deployment demonstration, test plans)
- Held GSE software peer review (and IDPU flight software status)
- Participated in EMC and Contamination Control Committee telecons
- Participated in Actel current spike discussions and testing
- Performed SEP/SEPT ETU integration test at Caltech

1.3. *System Design Updates*

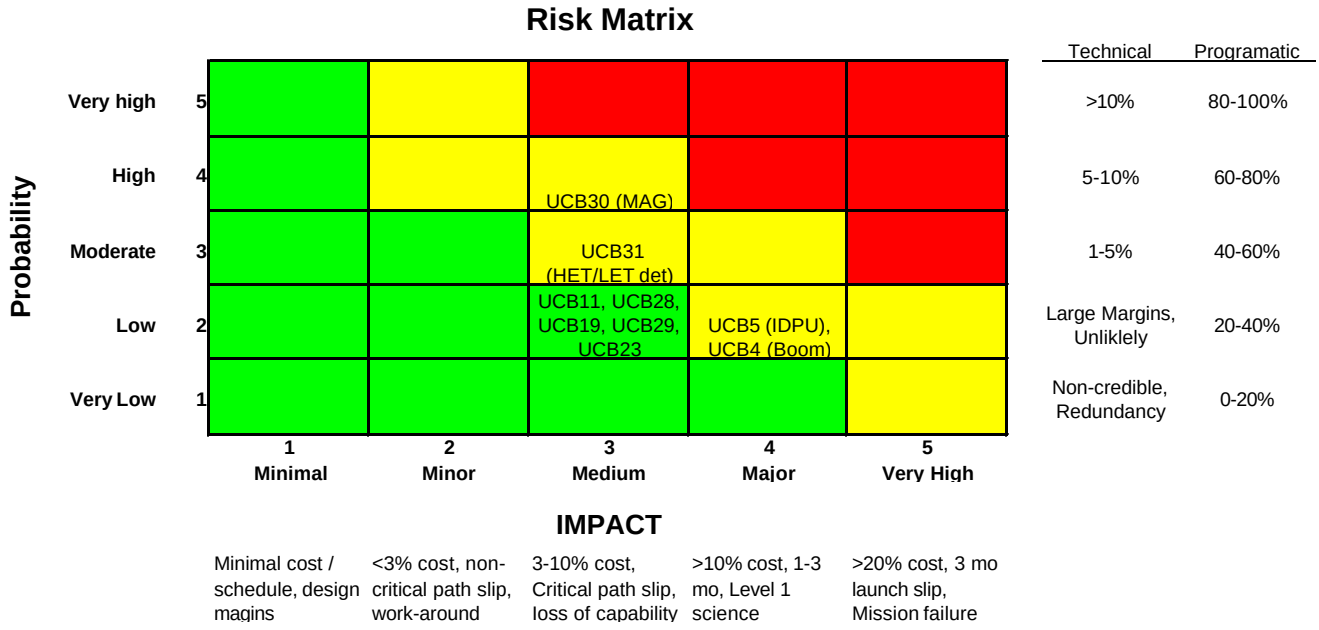
- None

1.4. *System Outstanding Issues*

- SEPT proton energy threshold not meeting requirement due to extra aluminum deposited to improve stray light rejection. Waiver submitted
- HET/LET detector adhesive material (outgassing) waiver submitted. Approved by Contamination Committee, submitted to CCR
- New boom cork contamination waiver submitted, pending test results.

1.5. *Top 10 Risks*

Top 10 risks are attached. No change from last month..


Risk Matrix
Probability
Very high 5
High 4
Moderate 3
Low 2
Very Low 1
UCB30 (MAG)
UCB31 (HET/LET det)
UCB11, UCB28, UCB19, UCB29, UCB23
UCB5 (IDPU), UCB4 (Boom)
1 Minimal
2 Minor
3 Medium
4 Major
5 Very High
IMPACT
Technical
Programatic
>10%
80-100%
5-10%
60-80%
1-5%
40-60%
Large Margins, Unliklely
20-40%
Non-credible, Redundancy
0-20%
Minimal cost / schedule, design magins
<3% cost, non-critical path slip, work-around
3-10% cost, Critical path slip, loss of capability
>10% cost, 1-3 mo, Level 1 science
>20% cost, 3 mo launch slip, Mission failure

IMPACT Top Ten Risks 4/2003

No.	Risk Item	Score	Mitigation	Mitigation Schedule						
				PDR	EM Test	CDR	Sub-system Test	System Test	Env test	Early Orbit Test
UCB_5	IMPACT boom is a new design. Failure could affect Imager pointing requirements as well as boom-mounted instruments.	MEDIUM	Design for reliability. Early prototype testing. Adequate force margins.	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	LOW
UCB_30	SECCHI magnetics (especially filter wheen motor) may exceed magnetics requirement, impacting MAG science	MEDIUM	Test to evaluate possible screening techniques; evaluate modeling capability if screening fails	MEDIUM	MEDIUM	MEDIUM	MEDIUM	LOW	LOW	LOW
UCB_4	The IDPU is a single point failure mechanisim for the IMPACT suite and PLASTIC	MEDIUM	IDPU is a simple, reliable system. Extra attention will be paid to ensuring its reliability, minimizing the risk of fault propagation. Early prototype testing; extensive FM testing	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM
UCB_31	HET/LET ETU detector mounting difficulties impacting schedule	MEDIUM	Idnetify and solve problems; bring in outside experts to evaluate process, continue with flight detector fab in parallel	MEDIUM	MEDIUM	MEDIUM	MEDIUM	LOW	LOW	LOW
UCB_23	Non-standard parts qualification failure could impact delivery schedule	LOW	Early parts selection and screening	MEDIUM	MEDIUM	MEDIUM	LOW	LOW	LOW	LOW
UCB_27	Actel timing differences between flight & ETU parts may cause failures late in testing impacting delivery schedule	LOW	Do FM Thermal Vac early to allow time for finding and fixing timing problems; for designs on the critical path, consider installing a flight Actel in the ETU & thermal cycle.	MEDIUM	MEDIUM	MEDIUM	LOW	LOW	LOW	LOW
UCB_11	Stringent EMI requirements may delay schedule if testing fails	LOW	Careful design, ETU power converter testing, early system testing	MEDIUM	MEDIUM	MEDIUM	LOW	LOW	LOW	LOW
UCB_28	Thermal limitations of detectors result in a low bakeout temperature which might require a very long bakeout impacting delivery schedule	LOW	Bakeout subsystems prior to detector integration to reduce time of instrument-level bakeout; early bakeout	MEDIUM	MEDIUM	MEDIUM	LOW	LOW	LOW	LOW
UCB_19	Concern about fragility of ITO surfaces required to meet ESC requirements; failure will impact SWEA science	LOW	Replace ITO with more robust solution where possible; test ITO surfaces during I&T and replace when required	MEDIUM	MEDIUM	MEDIUM	LOW	LOW	LOW	LOW
UCB_29	LVPS behind schedule, on critical path; further slipping could delay delivery to spacecraft	LOW	Add manpower to LVPS task to avoid further slippage	MEDIUM	MEDIUM	MEDIUM	MEDIUM	LOW	LOW	LOW

2. Berkeley Status

2.1. *Summary of Status*

Schedule status through June has been provided separately.

2.2. *Major Accomplishments*

SWEA/STE:

- Completed tests of SWEA/STE interface ETU.
- Integrated & tested SWEA/STE interface ETU with SWEA LVPS ETU
- Performed I&T of SWEA/STE interface ETU with IDPU ETU
- Performed I&T of SWEA/STE interface ETU with SWEA ETU
- STE ETU completed and tested. Test with SWEA/STE interface pending.

IDPU:

- Flight Software: Working on Build 3 for IMPACT.
- PLASTIC software Build #2.3 in progress, with a target delivery date of July for the IDPU/PLASTIC ETU interface test.

LVPS/HVPS:

- SIT HVPS FM #1 build near completion (problem with shield wall PWB in work)
- SWEA/STE LVPS ETU delivered, tested with SWEA/STE interface
- PLASTIC LVPS ETU built, in test. SEE test of PWM has hit logistical problems.
- SEP LVPS layout complete, boards being fabricated

Boom:

- Qual Boom in integration, tested, some final adjustments made, ready to start qualification tests..
- Boom thermal-vac chamber built up and tested (vacuum part). Thermal shroud and controller in work.

GSE:

- Continued additions to C&T GSE, SWEA/STE GSE.

2.3. *Design Updates*

- None.

2.4. *Outstanding Problems*

2.5. *New Problems*

2.6. *Top Risks.*

- Possible ELDR testing requirement
- LVPS schedule tight
- New Actel current spike problem may require changes to LVPS

2.7. *Problem/Failure Quick Look*

None.

3. GSFC (SEP) Status

STEREO/IMPACT/SEP/GSFC Progress Report for June, 2003 – (von Rosenvinge, Baker, Hawk, Reames, Shuman, Wortman)

3.1. *Summary of Status*

See below.

3.2. *Major Accomplishments*

HET PC-board (Engineering Test Unit) was delivered to Caltech for an interface test with SEP Central in mid-June. The HET MISC correctly booted up, downloading its code from SEP Central, correctly received commands, and correctly echoed them back. The board was then returned to GSFC for further testing prior to completing the design of the HET flight boards.

New L2 detector mounts have been received. These are being coupon-tested and mechanically inspected, following which flight connectors will be added so that the mounts can be sent to Micron no later than the end of July. New H3 detectors were also ordered, but 2 errors were made in the manufacture. We are investigating whether they can be salvaged instead of being remade. New H1 detector mounts have also been ordered. They are due on July 18. Twenty L1 detectors have had new connectors added and will be shipped to Micron soon. We have discovered that the flex-strip on the L1 mounts should have been 5.5 mm shorter than they were built to be. This error resulted when a revised connector location was reflected into the LET housing design and the detectors shown there but was not reflected in the drawings from which the mount was actually built. It's too late to modify the mounts, so we are working on revising the LET housing design to accommodate the added length. An estimated 55 g of additional weight may be required.

Completed EM LVPS box design. UCB is requesting .090" walls to provide additional radiation shielding. The weight impact has not yet been determined. The LET housing design continued to evolve.

Fabrication of flight mechanical parts began with shields for the High Voltage Bias Supply.

Tom Nolan and George Winkert have been assisting Peter Walpole at the University of Maryland with testing the SIT engineering unit. Tom is responsible, together with Kristin Wortman, for the on-board software and George implemented the SIT front-end logic and MISC on an ACTEL chip. SIT will be taken to Caltech by Peter Walpole for its interface tests during the coming month.

Capacitance versus voltage curves and leakage current versus voltage curves have been taken for all the prototype detectors. We are now working on taking 241Am spectra for all the prototypes. The two L3 prototypes were sent to Caltech to be scanned to make sure that they are depleting all the way to their edges.

Next Month-

Process new H1, H3, and L2 mounts and ship to Micron.
Update ICD with APL to include mounting hole diameters and correct LET FOV.
Make modifications to the LET housing to accommodate the L1 mounts.
Update mass of SEP Main.
Complete testing of HET ETU, make design modifications for the HET flight unit, and continue associated software development. A software development review for both HET and SIT is scheduled at GSFC for July 24.
Complete thermal blanket definition.
Work on defining the HET and SEPT radioactive sources to be supplied by GSFC.

3.3. *Design Updates*

Need to update mass of SEP Main.
MISC power consumption needs to be better defined when using the flight ACTEL chips (these have triple-redundancy gate-voting and consume roughly twice the power of the commercial equivalent part).

3.4. *Outstanding Problems*

3.5. *New Problems*

The choice of thermal blanket materials is being revisited because of manufacturability problems. The thermal design of the SIT sun-shade is being evolved.

3.6. *Top Risks*

No significant risks at GSFC? Need to ensure that manpower becomes available per the current plan.
We are running somewhat behind schedule with respect to detectors and the HET final electronics design.

3.7. *Problem/Failure Quick Look*

4. Kiel/ESTEC (SEPT) Status

June 2003

4.1. *Summary of Status*

1. SEPT milestone for June 2003 completed on time: ETU interface test with SEP Central was successful.
2. Procurement activities for flight parts nearly 100 % complete.
3. Schedule update statused for end of June. Kiel has no info on status of bracket design/manufacturing.
4. Waiting for the ETU interface test (to enable implementation of any changes which might result for flight units) introduced some delay, which can be absorbed without affecting delivery.

4.2. *Major Accomplishments*

a) Interface tests at Caltech completed. A SEPT "User Manual" will be produced by Caltech and reviewed by SEPT team for completion of the software.
b) Detailed Engineering Model tests at ESTEC.
c) Comprehensive Engineering Model test report is being written at ESTEC.
d) TID of the new PDFE design completed. Reports are in progress.
e) PA/QA: flight coupon of the analog board sent to R. Jackson.
f) Procurement: nearly all parts and materials inhouse. PDFE flight lot will be delivered in week 28. Final assembly of Canberra flight detectors in progress, delivery of first batch expected in July.
g) Mechanical work on sensor housing and electronics box in progress. Electronics box will be finished before vacation period starts. Finishing sensor housing on time needs still some arm-twisting.

4.3. *Design Updates*

4.4. *Outstanding Problems*

4.5. *New Problems*

1. Delay in the assembly of the first FM digital board to take into account any possible changes arising from the ETU interface tests at Caltech. No modifications required eventually. However an error has been reported in the footprint for the crystal on the FM digital board. This error has required an additional study to find a technical solution to avoid new board manufacturing: a custom stand-off will be manufactured at ESTEC, the solution is fully conform to ESTEC PA plan. The delay will be absorbed with no impact on delivery of the first flight models.
2. Procurement of the thermal coating (MSA94B) from Swales Aerospace poses some problems (looks like ITAR-induced). Sandy Shuman offered help. If delivered by mid August, no schedule problems will result.

4.6. *Top Risks*

4.7. *Problem/Failure Quick Look*

5. Caltech/JPL (SEP) Status

5.1. *Summary of Status*

Activities centered on detector development, electronics development, and flight and GSE software development.

5.1.1. Critical Milestones status:

There is some confusion about the milestone dates in some cases. The current schedule we are working to at Caltech is called LET.SEP.post03.01.31_03.02.18.mpp, which was created in February 2003. (There is a table of electronic board milestones called LET.SEP_Central.xls, which has some further schedule mods for board production; those are not involved in the following discussion, except for Milestone 13.) The milestone dates in the IMPACT Critical Milestone Chart of 4/30/03 don't always agree with the current Caltech schedule. So, in the below status I will call out two planned dates. The Milestone Chart date of 4/30/03 will be prefixed with the letter M. The Caltech schedule date will be prefixed with the letter C.

- Milestone 16 (SEPT-Deliver ETU to CIT) of the IMPACT Critical Milestones chart dated 4/30/03 was accomplished on 6/11/03. (Planned: M 6/11/03; C 6/24/03)
- Milestone 14 (HET – Deliver EM to CIT) was accomplished on 6/19/03. (Planned: M 5/13/03; C 7/8/03).
- Milestone 13 (SEP-ETU LVPS Available) has yet to be accomplished. (Planned: M 5/5/03; C 5/5/03; new 7/8/03 plan: 8/21/03). We have not been losing schedule time due to this late delivery as we are using bench supplies to substitute for the LVPS.

5.2. *Major Accomplishments:*

Detectors:

- The thermal-vacuum life test of six L1 detectors (3 of the membrane devices and 3 of the thick/thin version) is nearing completion. No indication of instability has been found in any of these detectors. This run will be ended in early July another run started for the other 6 more L1 detectors that we presently have.
- Thickness maps were made of the 6 L1 detectors that were not in the thermal vacuum run. The mean thicknesses of the 3 detectors made from lapped and polished wafers were larger than expected, 28-30 microns rather than the nominal 18-22 microns. When asked about this, Micron Semiconductor checked the paper work that came from the wafer polishing company (Virginia Semiconductor) and also measured some scrap pieces from the wafers used to make the detectors. They concur that the wafers were close to 30 microns thick, although the paper work said they were in the nominal 18-22 micron range. Micron followed up by measuring some wafers subsequently received from Virginia Semiconductor and they report that the new wafers are close to the desired 20 microns. The thickness uniformity of the detectors made from lapped and polished wafers was fine.
- The three prototype L1 detectors made from thick wafers etched down to the desired thickness over the active area had absolute thicknesses closer to the desired 20 microns, but had significant thickness non-uniformities on both large and small scales. It is thought that the non-uniformities may be due to insufficient stirring of the KOH during the etching process. Since etched L1 detectors are no longer the baseline for flight and since the production of L1s from lapped and polished wafers appears to be

making good progress, we are deferring further investigation of the thickness properties of the etched L1 until there is a break in our other testing activities.

Electronics:

- The effort toward installing a functional "flight" Actel FPGA in our SEP Central Logic board continued. After a thorough investigation revealed that the failure of one flight Actel (which burned OK but failed to perform properly) was actually due to a faulty Actel part (rather than design marginality), we burned another flight Actel using the same fuse file. That one worked perfectly up to about 11 MHz. (The earlier "failed" one worked perfectly only below 8/3 MHz.) The power consumption of the "flight" part relative to the commercial one generated from the same layout was found to be only about 50% higher on the 2.5V supply and the same on the 3.3V supply. This is much less of an increase than the factor of 3 anticipated on the 2.5V supply.
- However, the detailed timing studies performed during the problem investigation showed that for adequate margin over worst case conditions we should reduce the clock rate for the MISCs from 8 MHz to 6.4 MHz. Our MISC clock is generated within the Actel from a 32 MHz externally supplied clock. 6.4 MHz is obtained by dividing that clock by 5 rather than 4. The clock is now asymmetrical, with the 3/5 duty cycle for the high state chosen to increase timing margin where most needed.
- We are preparing for the flight fab of the SEP Central logic board.
- The fab of the LET Front-end/MISC rigid-flex assembly was delayed both in the layout at Caltech and in the setup at the PCB vendor, but is now in fab with due date of July 25. To avoid delay in the other aspects of LET development, the design of the LET MISC Actel is proceeding using the PHASIC hybrid test fixture as a development platform. That design is now about 90% complete, and includes a FIFO implemented within the Actel to reduce front-end dead time. The LET flight software has also moved forward in support of the MISC Actel development. Basic hardware interface routines are working and test pulser data can move through the FIFO and into the MISC. PHASIC setup and operation software have been carried over with little modification from that used in the PHASIC hybrid tester. (Details of the design changes relative to the designs used in the PHASIC tester will be forwarded to GSFC soon. The general nature of the changes has already been sent by e-mail.)
- Experience with the flight software development for the SEP Central MISC indicated that the original allocation of parameter and return stack depth within the MISC design needed adjustment. The original depths of 16 and 32 for parameter and return stack respectively were altered to 24 and 24, which provides a balanced amount of margin (near 8 in both cases) for the SEP Central code. This new allocation will also be used in the LET MISC.
- I/F test between SEPT and SEP Central electronics was performed successfully. Both SEPT ETU and SEPT advanced breadboard unit were integrated with SEP Central Logic and Analog/Post-Reg boards using flight-like ETU harness built by JPL.
- Production of flight PHASIC hybrids continued at JPL. Eight devices were fabricated and delivered to Caltech for initial room temperature electrical test. Seven units passed the test and at least three of them are perfect (all 16 channels working at both low and high gain).
- Completed temperature tests for Bias Supplies. Tests included room, +55 degree C and - 40 degree C. Power supplies were loaded using resistive loads for no load and full load conditions. All tests were OK.

- Still need a set of capacitive loads for each detector with which to load the bias supplies. Then the tests will be re-run simulating actual loads including capacitive loads.
- Completed room temperature tests for Analog/Post-Regulator board. All tests were OK. Planning to complete the temperature tests early July.

Software:

- Worked on LET onboard data processing algorithms.
- Worked on improvements to PHASIC testing software.

GSE:

- Added temporary data capture software to the SEP GSE for the HET/SEP interface test.
- Participated in the HET/SEP interface test. HET telemetry was successfully passed to the SEP GSE, displayed on the SEP GSE (HEX dumps only), and captured to the SEP GSE disk. The packets captured during the interface test were sent to GSFC (via ftp) for further analysis. GSFC reported some success in capturing the telemetry remotely. The ability to send commands from the HET GSE via the SEP GSE was not tested.
- Partially completed the low level software needed to display scatter plots of LET events. (Software to analyze the LET events to generate the arrays of data for the scatter plot has not begun.)

5.3. *Design Updates*

- Resource updates will be sent separately.

5.4. *Outstanding Problems*

- Two flight Actels have failed; one failed to program and one is not functioning properly after programming. Problems are being reviewed with Actel.
- All detector mounts, except L1, are being remade due to various problems. Schedule impact on delivery of flight detectors is being worked with Micron.

5.5. *New Problems*

- None

5.6. *Top Risks.*

- The budget is very tight with no reserve being held at Caltech.

5.7. *Problem/Failure Quick Look*

- None.

6. SIT MONTHLY TECHNICAL PROGRESS REPORT

6.1. *SUMMARY of STATUS*

a. SIT TELESCOPE - Prototype is in house and working. Flight solid state detectors are in house, awaiting test. Flight Microchannel plates are in house and testing has begun.
b. SIT TOF System - FM1 has been downgraded to ETU and returned to UMd. Work is proceeding at MPAe to generate a new FM1 and FM2.
c. SIT Energy/Logic System – ETU Energy system, ETU TOF system and the ETU motherboard have been integrated with the ETU Logic system including front-end logic and MISC. Testing is underway at Umd.
d. SIT HVPS - Flight HVPS ETU is being built at UCB.

6.1.1. Schedule Changes

The current SIT schedule is available from David Rowse

6.2. *MAJOR ACCOMPLISHMENTS*

6.2.1. This Month

Motherboard: The ETU motherboard was completed and cabled to the computer.

Logic: ETU logic board was assembled

GSE: Necessary serial ports were installed in the GSE computer. Software infrastructure (communication S/W to the MISC, MISC assembler and the first cut at the flight code) were installed. Silicon Explorer – a tool for examining nets inside the ACTEL - was installed and probe files for the MISC Actel were downloaded.

Logic: The ETU Logic board with MISC was assembled and the MISC was received from George Winkert and installed. The complete ETU system was powered up and troubleshooting was begun. By the end of the month, connection problems had been resolved and the Actel was no longer stuck in Reset, but code testing had not begun.

Detectors: MCP testing continued

6.2.2. Next Month

Next month we intend to get a version of the flight code operating in the MISC and perform the interface test with the CDPU at Caltech.

6.3. *DESIGN UPDATES*

6.3.1. Resources

	Last Month	This Month	Change
Mass (kg) *	1.46	1.46	0
Power (W)	1.36	1.56	0.2
Telemetry (bps)	418	418	0

* Includes 200g book-kept by GSFC for SIT structure
A new estimate of Actel power for the flight units indicates that power will increase. Previous estimates had neglected the effect of the triple gates in the flight units for single-event upset protection.

6.4. *OUTSTANDING PROBLEMS*

We are continuing to work TOF parts issues.

6.5. *NEW PROBLEMS*

6.6. *NEW RISKS*

6.7. *PROBLEM/FAILURE QUICK LOOK*

Starts at first turn-on of flight hardware.

ID #	Description	Assignee	Opened	Closed

7. CESR (SWEA) Status

CESR- TOULOUSE- France **Author : Claude Aoustin / Project Manager**

SWEA PROGRESS REPORT # 21
(July 15, 2003)

June 2003

CESR is in charge of :

- Electrostatic analyzer with deflectors, grids and Retractable Cover
- Detector consisting of two MCP rings
- Amplifiers and discriminators
- 3 High voltages

7.1. *Summary of Status*

7.1.1. ETU1

Delivery to UCB was planned for 12/07/2002 : done 26/09/2002

7.1.2. ETU2

Mechanical fabrication 100 % done

Integration done for the vacuum test configuration.

Electronic boards tested (100 %).

7.1.3. FM1 / FM2

Mechanical fabrication 95 % done.

Grids under fabrication. Delivery planned end of July for FM1.

Surface treatment of the analyzer spheres done.

Surface treatment (gold, alodine) done.

Pin Puller integrated and tested.

Electronics boards fabrication :

Done for HV coupling board

Done for amplifiers board

Done for the HV board

7.2. *Major accomplishments*

Mechanical fabrication completed for FM1 and 2 except the grids.

HV coupling and amplifiers board populated and tested.

HV board: populated and tested

Final integration on the way.

Verification under vacuum for FM1 will start around the 20 of July.

7.3. *Design Updates*

Mass : 1040 g (EM is 950g without cover opening mechanism)

Power : 446 mW min ; 662 mW max

7.4. *Outstanding Problems*

Answer to comments on parts list sent. Still some answers to be clarified. Telecon planned at the end of July.
Answer to comments on materials list sent.
Additional heater (0.5 watts) requested by the project. Is it still true ?

7.5. *New problems*

None

7.6. *Top Risks*

7.7. *Problem Failure Quick Look*

None

8. GSFC (MAG) Status

ETU#2 MAG fabrication completed, started testing.

9. EPO at UCB

Monthly E/PO Report June, 2003

Formal Education:

We have finished the first draft of the magnetism and IMPACT boom lesson. The lesson is being read by people in the E/PO community, the IMPACT PI, Janet Luhmann, and middle and high school teachers.

We continued to organize a Teacher PD workshop at the SSL on July 19th, following the Lawrence Hall Science GEMS workshop. So far 15 teachers have signed up for the workshop.

Informal Education:

L. Peticolas submitted an abstract to the Space Weather Education and Public Outreach Conference that takes place as part of the American Meteorolo gy Society in Seattle, WA in January, 2004. The abstract is titled: "Space weather education using sounds from data and visualizations from simulations" with the following co-authors: L. M. Peticolas, J. G. Luhmann, W. P. Abbett, N. Craig, B. J. Mendez, and I. Sircar.

Public Outreach:

"News and Events" 2003 IMPACT web page updated.

Cross Cutting:

L. Peticolas, N. Craig, and B. Mendez met with J. Luhmann to discuss the various IMPACT E/PO projects. Mostly the IMPACT sounds project was discussed and it was decided that to begin with L. Peticolas would work with J. Luhmann to turn more Helios data into sound. Then a web page will be designed so that people can try out their own simple mapping from data to sound. We also discussed that it might make sense to hire Marty Quinn to do some of the sounds work for us since he has worked with the New Hampshire group and many others in successful sounds projects.

STEREO Mission:

We are still trying to help with the STEREO visualization/video project. B. Abbett and L. Peticolas have been in contact with the Goddard visualization lead, Tom Bridgeman. B. Abbett sent along simulation data of an active solar region that will hopefully be used in a 3-D visualization project for STEREO.

L. Peticolas has begun to discuss with J. Luhmann how to collaborate with the SECEF-Exploratorium IDEAS group in terms of creating STEREO visualizations that can be used in the above mentioned STEREO project and in the IMPACT sounds project.

Respectfully Submitted,
IMPACT E/PO scientists Nahide Craig, Laura Peticolas