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Subject: IMPACT Monthly Technical Progress Report, Contract NAS5-00133

Lil:

Enclosed is the monthly technical progress report for the STEREO IMPACT project for the month of May 2003.

Sincerely,

David Curtis
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CC:

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IMPACT Team

1. IMPACT Overview

This report is presented in sections by institution. Section 1 is an IMPACT Project Manager / System Engineer's overview.

1.1. *Contracting / Funding*

Funding through the end of FY03 seems to be in the pipes. Because of pipe-line delays in the system through to the subcontractors (Caltech and UMd) it is important that IMPACT be funded somewhat in advance of expected spending. There is some concern over the pending financial services shutdown at GSFC, particularly for the GSFC team members. Even with the best planning there will be unexpected needs during this interval that could threaten our schedule.

A new budget plan for IMPACT has been agreed upon that fits within the funding constraints without sacrificing hardware. Some pre-launch science support has been cut, but development of level 1 data reduction software has been maintained. An official version of this budget is being submitted for a contract mod.

1.2. *Significant System-Level Accomplishments*

- Participated in EMC and Contamination Control Committee meetings at APL
- Participated in an IMPACT/SWAVES I&T meeting at APL and telecon
- Participated in Actel current spike discussions and testing
- Participated in SECCHI Magnetics issue discussions following testing last month
- Performed SEP to IDPU ETU Interface Test

1.3. *System Design Updates*

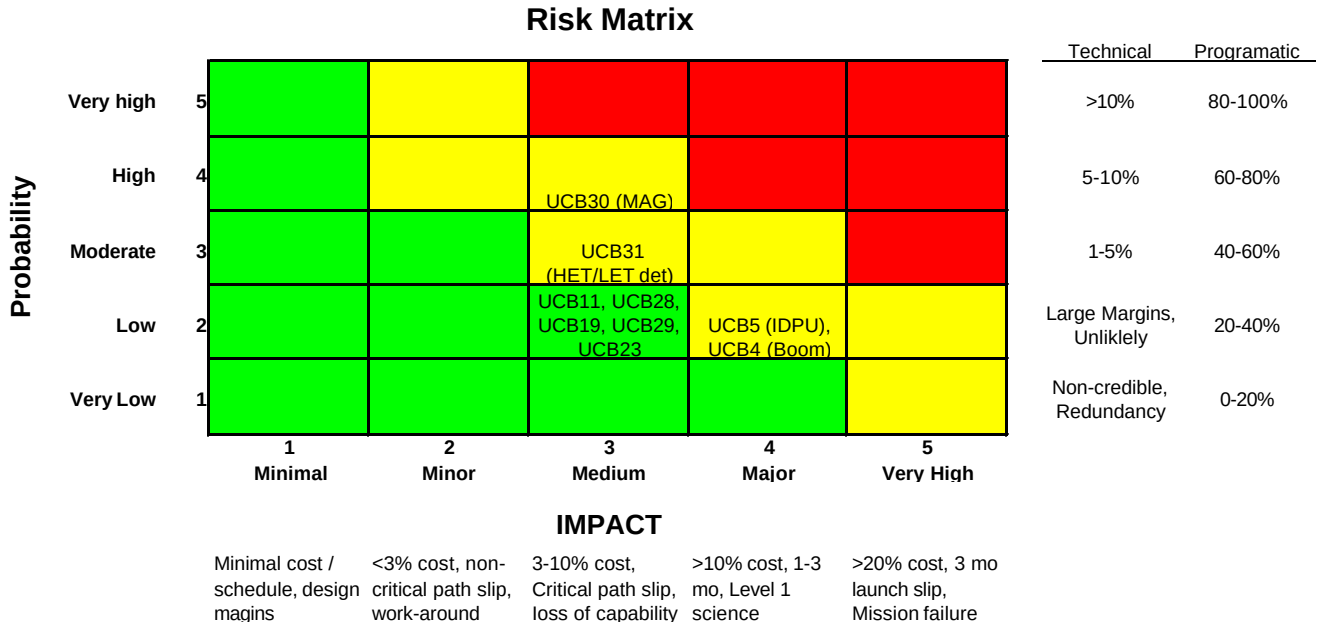
- None

1.4. *System Outstanding Issues*

- SEPT proton energy threshold not meeting requirement due to extra aluminum deposited to improve stray light rejection. Waiver submitted
- HET/LET detector adhesive material (outgassing) waiver submitted. Approved by Contamination Committee, submitted to CCR
- New boom cork contamination waiver submitted, pending test results.

1.5. *Top 10 Risks*

Top 10 risks are attached. The Actel current spike problem is a new risk, though not a high-level one for IMPACT (not in the top 10), as we do not expect the work-around costs to be too large.


Risk Matrix
Probability
Very high 5
High 4
Moderate 3
Low 2
Very Low 1
UCB30 (MAG)
UCB31 (HET/LET det)
UCB11, UCB28, UCB19, UCB29, UCB23
UCB5 (IDPU), UCB4 (Boom)
1 Minimal
2 Minor
3 Medium
4 Major
5 Very High
IMPACT
Minimal cost / schedule, design magins
<3% cost, non-critical path slip, work-around
3-10% cost, Critical path slip, loss of capability
>10% cost, 1-3 mo, Level 1 science
>20% cost, 3 mo launch slip, Mission failure
Technical
Programatic
>10%
80-100%
5-10%
60-80%
1-5%
40-60%
Large Margins, Unliklely
20-40%
Non-credible, Redundancy
0-20%

IMPACT Top Ten Risks 4/2003

No.	Risk Item	Score	Mitigation	Mitigation Schedule						
				PDR	EM Test	CDR	Sub-system Test	System Test	Env test	Early Orbit Test
UCB_5	IMPACT boom is a new design. Failure could affect Imager pointing requirements as well as boom-mounted instruments.	MEDIUM	Design for reliability. Early prototype testing. Adequate force margins.	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	LOW
UCB_30	SECCHI magnetics (especially filter wheen motor) may exceed magnetics requirement, impacting MAG science	MEDIUM	Test to evaluate possible screening techniques; evaluate modeling capability if screening fails	MEDIUM	MEDIUM	MEDIUM	MEDIUM	LOW	LOW	LOW
UCB_4	The IDPU is a single point failure mechanisim for the IMPACT suite and PLASTIC	MEDIUM	IDPU is a simple, reliable system. Extra attention will be paid to ensuring its reliability, minimizing the risk of fault propagation. Early prototype testing; extensive FM testing	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM
UCB_31	HET/LET ETU detector mounting difficulties impacting schedule	MEDIUM	Idnetify and solve problems; bring in outside experts to evaluate process, continue with flight detector fab in parallel	MEDIUM	MEDIUM	MEDIUM	MEDIUM	LOW	LOW	LOW
UCB_23	Non-standard parts qualification failure could impact delivery schedule	LOW	Early parts selection and screening	MEDIUM	MEDIUM	MEDIUM	LOW	LOW	LOW	LOW
UCB_27	Actel timing differences between flight & ETU parts may cause failures late in testing impacting delivery schedule	LOW	Do FM Thermal Vac early to allow time for finding and fixing timing problems; for designs on the critical path, consider installing a flight Actel in the ETU & thermal cycle.	MEDIUM	MEDIUM	MEDIUM	LOW	LOW	LOW	LOW
UCB_11	Stringent EMI requirements may delay schedule if testing fails	LOW	Careful design, ETU power converter testing, early system testing	MEDIUM	MEDIUM	MEDIUM	LOW	LOW	LOW	LOW
UCB_28	Thermal limitations of detectors result in a low bakeout temperature which might require a very long bakeout impacting delivery schedule	LOW	Bakeout subsystems prior to detector integration to reduce time of instrument-level bakeout; early bakeout	MEDIUM	MEDIUM	MEDIUM	LOW	LOW	LOW	LOW
UCB_19	Concern about fragility of ITO surfaces required to meet ESC requirements; failure will impact SWEA science	LOW	Replace ITO with more robust solution where possible; test ITO surfaces during I&T and replace when required	MEDIUM	MEDIUM	MEDIUM	LOW	LOW	LOW	LOW
UCB_29	LVPS behind schedule, on critical path; further slipping could delay delivery to spacecraft	LOW	Add manpower to LVPS task to avoid further slippage	MEDIUM	MEDIUM	MEDIUM	MEDIUM	LOW	LOW	LOW

2. Berkeley Status

2.1. *Summary of Status*

Schedule status through May has been provided separately.

2.2. *Major Accomplishments*

SWEA/STE:

- Loaded revised Actel onto new SWEA/STE DAC board and started tests
- Continued tests of STE detector mounted to PWB. Measured light sensitivity of detector to verify it will not be swamped by starlight or scattered sunlight.

IDPU:

- Flight Software: Working on Build 3 for IMPACT.
- PLASTIC software Build #2.3 in progress, with a target delivery date of July for the IDPU/PLASTIC ETU interface test.

LVPS/HVPS:

- SIT HVPS FM #1 build in progress (1 part short)
- SWEA/STE LVPS ETU delivered, pending tests with SWEA & STE
- PLASTIC LVPS ETU partially built, in test, preparing for SEE test of PWM
- SEP LVPS layout near completion.

Boom:

- Qual Boom in integration, nearly ready for first deployment.
- Still waiting of pin-puller delivery.
- Boom thermal-vac chamber being built up and tested.

GSE:

- Continued additions to C&T GSE, SWEA/STE GSE.

2.3. *Design Updates*

- None.

2.4. *Outstanding Problems*

2.5. *New Problems*

2.6. *Top Risks.*

- Possible ELDR testing requirement
- LVPS schedule tight
- New Actel current spike problem may require changes to LVPS

2.7. *Problem/Failure Quick Look*

None.

3. GSFC (SEP) Status

STEREO/IMPACT/SEP/GSFC Progress Report for May, 2003 – (von Rosenvinge, Baker, Hawk, Reames, Shuman, Wortman)

3.1. *Summary of Status*

See below.

3.2. *Major Accomplishments*

Worked on testing the HET PC-board (Engineering Test Unit). This has basically gone well, with miscellaneous minor problems having been identified. Solutions or temporary work-arounds have been found for each of these problems. This board was supposed to have been sent to Caltech for an interface test with SEP Central at the end of May. However this test has slipped to mid-June.

Received a total of 40 new L1 detector mounts. Of these about a third failed to meet mechanical specifications. Replacements have been delivered and have been submitted for mechanical inspection. These will have connectors added and then they will be shipped to Micron shortly. The soldering procedures for these connectors have been reviewed following the lifting of some pads from the H1 detector mounts. A deviation request to use water-soluble flux has been submitted and a Wahl's soldering iron tester has been purchased. A new solder pot for tinning has also been ordered. Cleaning of the mounts will be followed by a vacuum bakeout. It's not clear that any of these steps would have led to a different outcome for the H1 detectors, however.

New L2 and H3 detector mounts have been ordered. These will be coupon-tested, mechanically tested, and have flight connectors added so that they can be sent to Micron no later than the end of July. New H1 detector mounts have also been ordered.

The LVPS housing design has been iterated.

Completed defining the HET Stopping Particle Identification tables.

Delivered an ACTEL chip to the University of Maryland with a MISC and front-end logic for SIT. Corresponding on-board and GSE software will be delivered soon.

Worked on GSE software (dealing with CCSDS headers, supplemented command messages, connecting to the Caltech GSE via internet sockets, etc.).

3.2.1. Next Month-

Deliver HET ETU and preliminary HET software to Caltech for interface testing with SEP Central.
Ship new H1, H3, L1, and L2 detector mounts to Micron.

Update ICD with APL to include mounting hole diameters and correct LEMT FOV.
Complete LVPS and LET housing designs.
Update mass of SEP Main.
Deliver SIT on-board and GSE software to U of Maryland.
Complete testing of HET ETU, make design modifications for the HET flight unit, and continue associated software development.
Begin fabrication of various flight mechanical parts.
Complete thermal blanket definition.
Work on defining the HET and SEPT radioactive sources to be supplied by GSFC.

3.3. *Design Updates*

Need to update mass of SEP Main.
MISC power consumption needs to be better defined when using the flight ACTEL chips (these have triple-redundancy gate-voting and consume roughly twice the power of the commercial equivalent part).

3.4. *Outstanding Problems*

3.5. *New Problems*

The choice of thermal blanket materials is being revisited because of manufacturability problems. The thermal design of the SIT sun-shade is being evolved.

3.6. *Top Risks*

No significant risks at GSFC? Need to ensure that manpower becomes available per the current plan.

3.7. *Problem/Failure Quick Look*

4. Kiel/ESTEC (SEPT) Status

SEPT Monthly Technical Progress Report
May 2003

4.1. *Summary of Status*

1. Tests of ETU electronics with sensor partially completed. Ready for ETU interface test with SEP Central in June.
2. There was a request for a waiver from the Printca company (Denmark) for the analog board. The test coupons and the PCBs have gone through the "Materials Mechanics and Processes" Section at ESTEC for verification. The waiver was accepted and the PCB declared okay for flight. We will send the test coupons to R. Jackson together with the internal report for approval.
3. Dedicated GSE power supply not yet delivered. Interface test with SEP Central must use commercial power supplies.
4. Schedule update statused for end of May. Negative slack (-7 days) for FM SEPT delivery to CIT not critical.

4.2. *Major Accomplishments*

a) Fabrication of structural model completed. Wooden model will serve as mock-up for MLI tayloring. Will be shipped to GSFC (or APL?) in June.
b) PA/QA: flight coupon for the digital board approved, flight coupon for EMI shield sent to R. Jackson.
c) Procurement: Analog board flight PCB delivered, EMI shield PCB board delivered, Flight crystals delivered.
d) TID of the new PDFE design in progress, PDFE packaging of flight lot has started.
e) Updated version of the SEPT Operation Control and Data processing requirements v3.0 delivered.

4.3. *Design Updates*

4.4. *Outstanding Problems*

4.5. *New Problems*

4.6. *Top Risks*

4.7. *Problem/Failure Quick Look*

5. Caltech/JPL (SEP) Status

5.1. *Summary of Status*

Activities centered on detector development, electronics development, and flight and GSE software development.

Major Accomplishments:

Critical Milestones:

- Milestone 13 (SEP-ETU LVPS Available) of the IMPACT Critical Milestones chart dated 2/28/03 was missed. Work continued unimpeded at Caltech using bench supplies. A new LVPS compatibility test is envisioned when all the ETU boards are available. This new task is being worked into the schedule; the overall schedule is not expected to slip.
- Milestone 14 (HET – Deliver EM to CIT) was missed. However, in its place Caltech delivered a second SEP Central logic board to GSFC to use for the interface test. It is still planned that the HET board will be delivered to Caltech for a double-check in June or July. The overall schedule is not impacted at Caltech.

Detectors:

- Micron Semiconductor has received 35 silicon wafers lapped and polished to 20-micron thickness by Virginia Semiconductor. Micron had sent 300 thick wafers to Virginia Semiconductor and thus far Virginia has processed 225 of these. Thus, as expected, the yield from the lapping and polishing process is relatively poor. Virginia will proceed with processing the remaining 75 wafers. Micron also received an initial quantity (approximately 50) of 30-micron lapped and polished wafers from Virginia.
- Micron has started L1 detector fabrication on 6 of the 20-micron wafers and 2 of the 30-micron wafers. (At present we have not placed an order for 30 micron detectors, but Micron decided to go ahead on their own with processing a few of these thicker wafers in order to avoid the start-up delay that would be incurred should we come to the conclusion that 30 micron detectors are needed.) For the L1 fabrication, 4 devices are produced on each of the 3-inch diameter wafers.
- The new wafers have resistivities of approximately 1200 to 1400 ohm-cm, rather than the 4000 ohm-cm used for some of the first detectors that were delivered. Micron believes that this will allow operation at somewhat higher bias voltage for optimizing charge collection.
- The thermal-vacuum life test of six L1 detectors (3 of the membrane devices and 3 of the thick/thin version) was started at Caltech. This set of detectors, which contains half of the L1s of each kind thus far received, should run until late June. During this time alpha particle measurements will be done on the remaining six detectors. During the thermal-vac test, leakage current and noise measurements are repeatedly made on each of the detectors to check for long-term stability. Most of the test is run near the high-end of the detectors' nominal operating temperature range.
- Micron is requesting feedback on the testing of the prototype H1, H3, L2, and L3 detectors. Once they hear that the performance of these devices looks ok they will begin manufacturing of flight detectors.

- GSFC is having mounts for detectors other than L1 remade for a variety of reasons. In early June we will be evaluating the impact of the mount re-manufacturing on the detector delivery and testing schedule.

Electronics:

- The main event was the interface test between our SEP Central Logic EM board and Berkeley's IDPU. The test went well, with both sides discovering a few easily fixable problems. The test included simulation of the SEP instrument suite (minus SEPT) so that simulated data, commands, and command responses were all flowing properly.
- We had less success in our efforts to successfully burn a "flight" Actel for SEP Central. In our first attempt the flight part failed to program at a certain fuse and Actel has agreed to provide an RMA. In our second attempt the part programmed ok, but only functioned properly when operated at one-third the desired 8 MHz frequency. At an intermediate frequency of 4 MHz the part operated adequately to boot our FORTH system and allow detailed diagnostics of the residual problem. The symptoms of the problem were specific enough to allow for only one possible explanation -- an excessive delay on the positive transition of a certain buffer, far in excess of the delay predicted by the Actel timer software. To verify that there was actually no problem with the design files, a commercial Actel was burned using the same routing files as used for the failed flight part. The commercial part worked perfectly, with 40% margin beyond 8 MHz and no evidence of the problem that had crippled the flight part's performance. So, unfortunately, it appears that there may be a quality problem with our flight Actels. The latter problem we encountered is particularly troublesome since the part programmed successfully, yet failed to function properly. This type of problem is extremely rare in our experience with commercial parts. Actel has been contacted and we will be working with them to investigate this failure further. In the meantime we will proceed to burn a third flight part using the same fuse file.
- While the flight part did not work perfectly, it did work well enough to yield an estimate of the rise in power to be expected in moving from the commercial to flight parts. We saw an increase in the 2.5-volt current of a factor of about 2, which is fortunately smaller than the factor of 3 we had been conservatively anticipating.
- In other progress, we completed a copy of the SEP Central Engineering board, checked in out and sent it to GSFC. That board was recently returned to Caltech to support an interface check with SEPT.
- Throughout the period, good progress continued on the flight software for SEP Central as needed to support the various interface tests. The support for HET, LET, SIT, and the IDPU interface is essentially complete while the software to operate SEPT is in progress.
- Some preparatory work was done toward the detailed design of the MISC Actel for the LET front-end/MISC EM board to be ready for test in early July.
- Fabrication of flight PHASIC hybrids began at JPL.
- Ahead S/C set of EM harnesses for SEPT-E/SEPT-NS/SIT fabricated by JPL.
- SEP thermal hardware sized and P/Ns defined for the purpose of common buy.
- Early I/F test performed between SEP Logic and Analog/Post-Reg boards. MDM connector layout mistake on the latter board discovered; it will be fixed by redefining pin-out on the flight harnesses, which haven't been built yet.
- LET rigid-flex board submitted for fabrication to Pioneer Circuits.
- Bias supply is assembled and tested at room temperature.

- Analog Board is assembled and 90% tested.
- Resource updates will be sent separately

Software:

- Worked on software development for SEPT sensor simulator.
- Worked on LET onboard data processing algorithms.
- Worked on improvements to PHASIC testing software.

GSE:

- Completed work on the software for the IMPACT/SEP logic board interface test. During the interface test there were no problems with the communication of the normal SEP telemetry between the SEP GSE and the IMPACT GSE. The transmission of SEP beacon data was not tested during this test since the IMPACT beacon packet was not defined at the time of the interface test. Since that time, the packet has been defined. On the commanding side, there were no problems in getting ASCII commands and moderately-long binary command loads from the SEP GSE to SEP via the IMPACT GSE. The procedure for uploading a new SEP kernel did not succeed. This was traced to limitations in the S/C emulator that was being used during the test. This issue has now been resolved.
- Added new software to the GSE for uploading EEPROM information for LET, HET, and SIT.
- Started work on the software for the HET/SEP logic board interface test in June. Have tested remotely with GSFC the transmission of telemetry packets between the SEP GSE and the HET GSE. On the commanding side, there are some problems in getting commands from the HET GSE to the SEP GSE; these problems are currently being worked.

5.2. *Design Updates*

- Resource updates will be sent separately.

5.3. *Outstanding Problems*

- None

5.4. *New Problems*

- Two flight Actels have failed; one failed to program and one is not functioning properly after programming. Problems are being reviewed with Actel.
- All detector mounts, except L1, are being remade due to various problems. Schedule impact on delivery of flight detectors is being worked with Micron.

5.5. *Top Risks.*

- The budget is very tight with no reserve being held at Caltech.
- Schedule slack that we show explicitly will be taken away from us.
- Development of the L1 detector. Risk mitigated by creating slack in schedule and by deciding to use more conventional manufacturing technique (Plan B detectors).

5.6. *Problem/Failure Quick Look*

- None.

6. SIT MONTHLY TECHNICAL PROGRESS REPORT

6.1. *SUMMARY of STATUS*

a SIT TELESCOPE - Prototype is in house and working. Flight solid state detectors are in house, awaiting test. Flight Microchannel plates are in house and testing has begun.

b SIT TOF System - FM1 has been downgraded to ETU and returned to UMd. Work is proceeding at MPAe to generate a new FM1 and FM2.

c SIT Energy/Logic System - Prototype energy system has been integrated with the prototype TOF system and is functioning at UMd. ETU energy system is completed and under test. Front-end logic has been implemented at GSFC and is under test at UMd. ETU logic with MISC is under construction at UMd.

d SIT HVPS - Flight HVPS ETU is being built at UCB.

6.1.1. Schedule Changes

The current SIT schedule is available from David Rowse

6.2. *MAJOR ACCOMPLISHMENTS*

6.2.1. This Month

- Energy: Flight board coupons were inspected. Half passed, half failed. The failed units have been removed from flight stock.
- Logic: ETU logic board design completed. Layout completed. Board was manufactured and assembled. Short was found and removed. ETU motherboard was laid out fabricated and parts ordered. We are working toward a working ETU unit in June for logic interface with the SEP central.
- Detectors: MCP testing continued

6.2.2. Next Month

We intend in June to begin testing ETU logic board with existing ETU energy and TOF boards. This will require an a completed motherboard and cable to the GSE, an ETU Actel, computer interface board, SIT MISC S/W and GSE software. The SIT software exists at GSFC but is untested. The GSE software is also at GSFC and is being used to test HET. The Actel is being developed at GSFC by George Winkert. The computer interface board will be built at UMd based on a GSFC Bob Baker design. The motherboard and cable will be produced at UMd. After testing at UMd, the ETU will be taken to Caltech for the logic interface test. We hope to begin assembly of flight energy boards.

6.3. *DESIGN UPDATES*

6.3.1. Resources

	Last Month	This Month	Change
Mass (kg) *	1.46	1.46	0
Power (W)	1.36	1.56	0.2
Telemetry (bps)	418	418	0

* Includes 200g book-kept by GSFC for SIT structure
A new estimate of Actel power for the flight units indicates that power will increase. Previous estimates had neglected the effect of the triple gates in the flight units for single-event upset protection.

6.4. *OUTSTANDING PROBLEMS*

We are continuing to work TOF parts issues.

6.5. *NEW PROBLEMS*

6.6. *NEW RISKS*

6.7. *PROBLEM/FAILURE QUICK LOOK*

Starts at first turn-on of flight hardware.

ID #	Description	Assignee	Opened	Closed

7. CESR (SWEA) Status

CESR- TOULOUSE- France **Author : Claude Aoustin / Project Manager**

SWEA PROGRESS REPORT # 20
(June 10, 2003)

May 2003

CESR is in charge of :
- Electrostatic analyzer with deflectors, grids and Retractable Cover
- Detector consisting of two MCP rings
- Amplifiers and discriminators
- 3 High voltages

7.1. *Summary of Status*

7.1.1. ETU1

Delivery to UCB was planned for 12/07/2002 : done 26/09/2002

7.1.2. ETU2

Mechanical fabrication 100 % done
Integration done for the vacuum test configuration.
Electronic boards tested (100 %).

7.1.3. FM1 / FM2

Mechanical fabrication 90 % done.
Surface treatment of the analyzer spheres done.
Surface treatment (gold, alodine) done.
Pin Puller integrated and tested.
Electronics boards fabrication :
Done for HV coupling board
Done for amplifiers board
Done for the HV board

7.2. *Major accomplishments*

Mechanical fabrication close to be completed.
HV coupling and amplifiers board populated : under test.
HV board : populated – under test

7.3. *Design Updates*

Mass : 1040 g (EM is 950g without cover opening mechanism)
Power : 446 mW min ; 662 mW max

7.4. *Outstanding Problems*

Answer to comments on parts list sent.
Answer to comments on materials list sent.
Additional heater (0.5 watts) requested by the project. Location to be defined.

7.5. *New problems*

None

7.6. *Top Risks*

7.7. *Problem Failure Quick Look*

None

8. GSFC (MAG) Status

Submitted revised part list
Mag analog PWB (potentially the flight boards) are in fabrication.

9. EPO at UCB

Monthly E/PO Report May, 2003

Formal Education:

L. Peticolas attended a professional development (PD) workshop at the Space Science Institute in Boulder, Colorado May 4-7. The workshop was called: "K-12 Education Workshop for Scientists, Engineers, and E/PO Professionals". It was about K-12 science education in the U.S. and how E/PO scientist can make the E/PO materials better suited for K-12 teachers and students.

We have continued work on our magnetism and IMPACT boom lesson. The boom lesson development continued. Pictures have been taken of the boom assembly, deployment of the engineering model, and the boom team members to be added to the lesson and the website. The teachers guide for the activities, including an introduction to the activities/lessons has been written. We are continuing to work on the background section of the guide as well as edits.

We have begun to organize a Teacher PD workshop at the SSL on July 19th, following the Lawrence Hall Science GEMS workshop. The Workshop opportunity announcement and other logistics will be arranged by the LHS. The IMPACT boom lesson activities as well as Magnetism lesson that is developed and other space weather related activities form the Living with a Star GEMS Guide will be used in this workshop. Peticolas and Mendez will be in charge.

Informal Education:

N. Craig gave a poster highlighting IMPACT E/PO activities at the American Astronomical Society meeting on May 26th in Nashville, Tennessee, titled "Education and Public Outreach Programs for RHESSI and STEREO/IMPACT Missions".

Public Outreach:

"News and Events" 2003 IMPACT web page updated.

Cross-Cutting:

Laura Peticolas is now the primary E/PO scientist for IMPACT and starting with this report, she will be in charge of the monthly reports, as well as developing IMPACT E/PO program advised by N. Craig. B. Mendez will be contributing to the UCB's Astrophysics Missions E/POs but will participate in IMPACT/EPO as time permits.

STEREO Mission:

We have begun to help organize a STEREO video project that would highlight the STEREO Mission and its science in a video/movie format. In order to get this project started, we have attended the MURI and CISM group meeting at the SSL to learn more about simulations of solar processes that might be able to be used in such a video. We also contacted the GSFC Visualization group, who are interested in using some of the MURI or CISM simulation data to make visualization for the STEREO mission. Don Michels and Evelina Felicite-Maurice are working on the same project and we plan to coordinate with them.

Respectfully Submitted,
IMPACT E/PO scientists Nahide Craig, Laura Peticolas