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Subject: IMPACT Monthly Technical Progress Report, Contract NAS5-00133

Lil:

Enclosed is the monthly technical progress report for the STEREO IMPACT project for the month of April 2003.

Sincerely,

David Curtis
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CC:

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IMPACT Team

# 1. IMPACT Overview

This report is presented in sections by institution. Section 1 is an IMPACT Project Manager / System Engineer's overview.

## 1.1. *Contracting / Funding*

Funding through the end of FY03 seems to be in the pipes. Because of pipe-line delays in the system through to the subcontractors (Caltech and UMd) it is important that IMPACT be funded somewhat in advance of expected spending. There is some concern over the pending financial services shutdown at GSFC, particularly for the GSFC team members. Even with the best planning there will be unexpected needs during this interval that could threaten our schedule.

A new budget plan for IMPACT has been agreed upon that fits within the funding constraints without sacrificing hardware. Some pre-launch science support has been cut, but development of level 1 data reduction software has been maintained.

## 1.2. *Significant System-Level Accomplishments*

- Participated in EMC and Contamination Control Committee telecons
- Participated in IIR review
- Presented HVPS manufacturing plan to review
- Worked IMPACT budget issues

## 1.3. *System Design Updates*

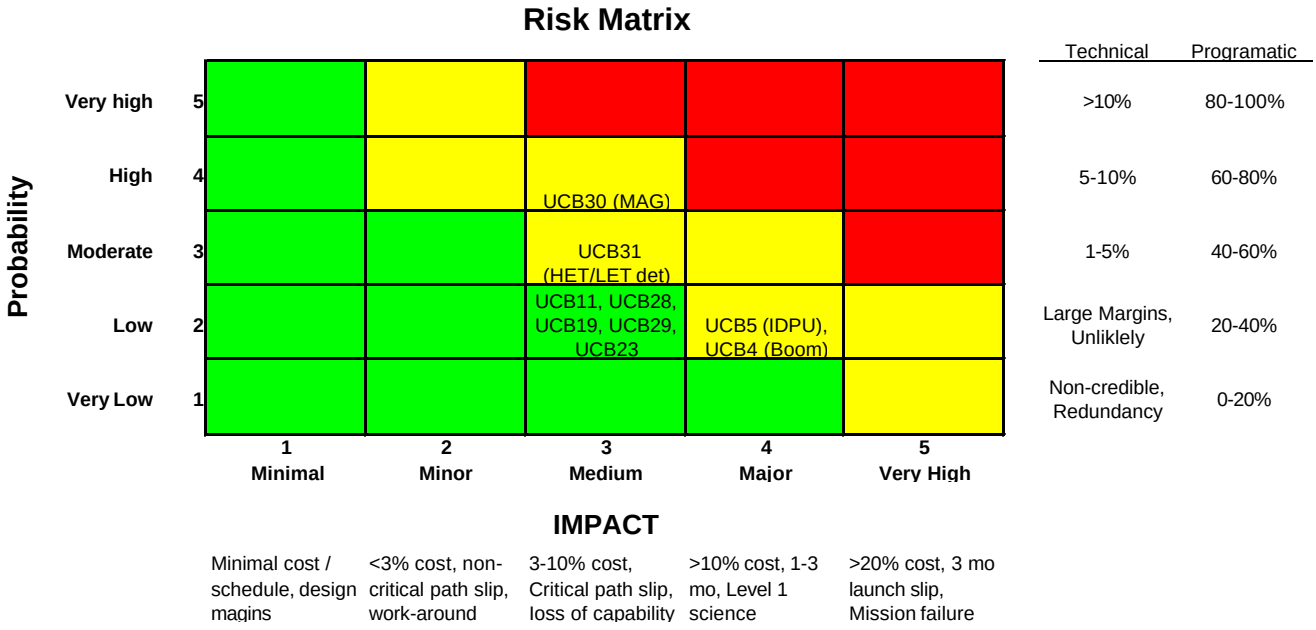
- None

## 1.4. *System Outstanding Issues*

- SEPT proton energy threshold not meeting requirement due to extra aluminum deposited to improve stray light rejection. Waiver submitted
- HET/LET detector adhesive material (outgassing) waiver submitted. Approved by Contamination Comittee.
- New boom cork contamination waiver submitted.

## 1.5. *Top 10 Risks*

Top 10 risks are attached. No significant changes this month..


Risk Matrix
Probability
Very high 5
High 4
Moderate 3
Low 2
Very Low 1
UCB30 (MAG)
UCB31 (HET/LET det)
UCB11, UCB28, UCB19, UCB29, UCB23
UCB5 (IDPU), UCB4 (Boom)
1 Minimal
2 Minor
3 Medium
4 Major
5 Very High
IMPACT
Technical
Programatic
>10%
80-100%
5-10%
60-80%
1-5%
40-60%
Large Margins, Unliklely
20-40%
Non-credible, Redundancy
0-20%
Minimal cost / schedule, design magins
<3% cost, non-critical path slip, work-around
3-10% cost, Critical path slip, loss of capability
>10% cost, 1-3 mo, Level 1 science
>20% cost, 3 mo launch slip, Mission failure

IMPACT Top Ten Risks 4/2003

| No. | Risk Item | Score | Mitigation | Mitigation Schedule | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | PDR | EM Test | CDR | Sub-system Test | System Test | Env test | Early Orbit Test |
| UCB_5 | IMPACT boom is a new design. Failure could affect Imager pointing requirements as well as boom-mounted instruments. | MEDIUM | Design for reliability. Early prototype testing. Adequate force margins. | MEDIUM | MEDIUM | MEDIUM | MEDIUM | MEDIUM | MEDIUM | LOW |
| UCB_30 | SECCHI magnetics (especially filter wheen motor) may exceed magnetics requirement, impacting MAG science | MEDIUM | Test to evaluate possible screening techniques; evaluate modeling capability if screening fails | MEDIUM | MEDIUM | MEDIUM | MEDIUM | LOW | LOW | LOW |
| UCB_4 | The IDPU is a single point failure mechanisim for the IMPACT suite and PLASTIC | MEDIUM | IDPU is a simple, reliable system. Extra attention will be paid to ensuring its reliability, minimizing the risk of fault propagation. Early prototype testing; extensive FM testing | MEDIUM | MEDIUM | MEDIUM | MEDIUM | MEDIUM | MEDIUM | MEDIUM |
| UCB_31 | HET/LET ETU detector mounting difficulties impacting schedule | MEDIUM | Idnetify and solve problems; bring in outside experts to evaluate process, continue with flight detector fab in parallel | MEDIUM | MEDIUM | MEDIUM | MEDIUM | LOW | LOW | LOW |
| UCB_23 | Non-standard parts qualification failure could impact delivery schedule | LOW | Early parts selection and screening | MEDIUM | MEDIUM | MEDIUM | LOW | LOW | LOW | LOW |
| UCB_27 | Actel timing differences between flight & ETU parts may cause failures late in testing impacting delivery schedule | LOW | Do FM Thermal Vac early to allow time for finding and fixing timing problems; for designs on the critical path, consider installing a flight Actel in the ETU & thermal cycle. | MEDIUM | MEDIUM | MEDIUM | LOW | LOW | LOW | LOW |
| UCB_11 | Stringent EMI requirements may delay schedule if testing fails | LOW | Careful design, ETU power converter testing, early system testing | MEDIUM | MEDIUM | MEDIUM | LOW | LOW | LOW | LOW |
| UCB_28 | Thermal limitations of detectors result in a low bakeout temperature which might require a very long bakeout impacting delivery schedule | LOW | Bakeout subsystems prior to detector integration to reduce time of instrument-level bakeout; early bakeout | MEDIUM | MEDIUM | MEDIUM | LOW | LOW | LOW | LOW |
| UCB_19 | Concern about fragility of ITO surfaces required to meet ESC requirements; failure will impact SWEA science | LOW | Replace ITO with more robust solution where possible; test ITO surfaces during I&T and replace when required | MEDIUM | MEDIUM | MEDIUM | LOW | LOW | LOW | LOW |
| UCB_29 | LVPS behind schedule, on critical path; further slipping could delay delivery to spacecraft | LOW | Add manpower to LVPS task to avoid further slippage | MEDIUM | MEDIUM | MEDIUM | MEDIUM | LOW | LOW | LOW |

# 2. Berkeley Status

## 2.1. *Summary of Status*

Schedule status through April has been provided separately.

## 2.2. *Major Accomplishments*

SWEA/STE:

- Fabricated & loaded new ETU DAC board
- Built & started tests on STE detector board
- Rebuilt STE ETU door mechanism with added actuator wire tensioner, completed life test
- Completed SWEA vacuum calibration tests with UCB SWEA/STE interface (old DAC board)

IDPU:

- Flight Software: Completed Build 2,
- PLASTIC software Build #2.3 in progress, with a target delivery date of July for the IDPU/PLASTIC ETU interface test.
- Built PWBs for flight DCB board, performed coupon tests

LVPS/HVPS:

- SIT HVPS PWBs fabricated, ready to load.
- SWEA/STE LVPS ETU PWB fabricated, loaded, in test
- PLASTIC LVPS ETU PWB fabricated, ready to load
- SEP LVPS layout started, on hold pending results from SWEA testing
- SWEA LVPS efficiency well below target, expecting SEP to also be below target. ~2.5W impact.

Boom:

- Last of the tubes delivered early May.
- Protoflight machined parts almost all completed, compatible with tube schedule
- Stacer in test, force at end of stroke looks significantly better than projected, improving force margin
- New pin-puller actuator behind schedule, available ~6/6. Early testing will be hand-actuated.
- Boom thermal-vac chamber parts on order, some have been delivered.

GSE:

- C&T GSE tested with SEP GSE (command & telemetry forwarding) in preparation for SEP/IDPU ETU test next month.

## 2.3. *Design Updates*

- None.

## 2.4. *Outstanding Problems*

## 2.5. *New Problems*

## 2.6. *Top Risks.*

- Possible ELDR testing requirement
- LVPS schedule tight

## 2.7. *Problem/Failure Quick Look*

None.

# 3. GSFC (SEP) Status

STEREO/IMPACT/SEP/GSFC Progress Report for March, 2003 – (von Rosenvinge, Baker, Hawk, Reames, Shuman, Wortman)

## 3.1. *Summary of Status*

The GSFC SEP schedule will be updated with the new Project scheduler in 2 days.

## 3.2. *Major Accomplishments*

- Completed fabrication and population of HET PC-board.
- Designed preliminary front-end logic for HET (part of the ACTEL chip which includes the MISC).
- Received two new L1 detector mounts (instead of 40! Due to a clerical error at the manufacturer. The remaining 38 are expected in the next several days.)
- Continued work on SEP commanding formats and other related issues.
- Received and inspected prototype L2, L3, H1, and H3 detectors (2 of each type). Found that the H3 detector wafers were too high in their mounts. The cause of this was traced to an upward cupping of ~ 15-20 mils of the shelf on which the detector wafer rests. The origin of this cupping has not been determined but new mounts will be ordered soon. The detector manufacturer has been alerted and no flight H3 detector wafers have been mounted.
- We received approval of our waiver request to use Shin-Etsu adhesive (KJR-9022E) in manufacture of SEP detectors.
- Revised L2 detector design so that the ohmic side is not in contact with mount. Also revised the connector end of the flex strip to eliminate trace peeling problem first encountered on the H1 detectors. The H3 detector mount is being similarly revised.
- The LVPS housing design is nearly complete. Some modifications were made to the LET housing design.
- Made considerable progress on defining the HET Particle Identification tables.

### 3.2.1. Next Month-

- Order new L2 and H3 detector mounts. Deliver L1 mounts to Micron.
- Update ICD with APL to include mounting hole diameters and correct LEMT FOV (this was delayed from last month due to having to make changes to the L2 and H3 detector mount designs).
- Complete LVPS and LET housing designs.
- Update mass of SEP Main.
- Deliver HET ETU and preliminary HET software to Caltech for interface testing with SEP Central.
- Complete testing of HET ETU and continue associated software development.
- Complete definition of the HET Particle Identification tables.
- Begin fabrication of various flight mechanical parts.
- Complete thermal blanket definition.
- Work on defining the HET and SEPT radioactive sources to be supplied by GSFC.

### 3.3. *Design Updates*

Need to update mass of SEP Main.
Have sent revised HET and SIT MISC power consumption figures to Caltech.

### 3.4. *Outstanding Problems*

We have still not received a contamination control plan from the Project. However we have discussed the requirements with Therese Errigo and are proceeding accordingly.

### 3.5. *New Problems*

The choice of thermal blanket materials is being revisited because of manufacturability problems.

### 3.6. *Top Risks*

No significant risks at GSFC? Need to ensure that manpower becomes available per the current plan.

### 3.7. *Problem/Failure Quick Look*

# 4. Kiel/ESTEC (SEPT) Status

**April 2003**

## 4.1. *Summary of Status*

1. Engineering model electronics delivered to Kiel according to schedule together with a preliminary GSE.
2. Fabrication of door mechanism for EM delayed. Does not affect ETU interface test with SEP Central.
3. Date and goal of interface test with SEP Central at Caltech agreed. This SEP milestone will be on schedule starting 11-June-03.

## 4.2. *Major Accomplishments*

a) Fabrication of flight model housing in progress. Ten items (out of 30) complete.
b) Set-up of preliminary GSE and power supply simulator in Kiel complete. All Okay.
c) Test of EM electronics with EM detector stack in progress. No serious problem areas identified.
d) Document "Calculations for a pin-puller driven unlatch system for a double lid" submitted to STEREO Project. This is the final report on the door deployment mechanism.
e) Document "STEREO SEPT Structural Analysis" complete and made available to Sandy Shumann, but not yet officially submitted, signature procedure pending.
f) Document "SEPT Operation Control and Data Processing Requirements" updating in progress.
g) Details of SEPT mounting lug design with Ultem bushings agreed with Sandy Shumann.
h) All outstanding action items from SEPT Door Peer Review closed.
i) SEPTschedule as of March 2003 (file SEPT.mpp) updated and delivered to Bob Palfy.
j) Mitigation technique for latchup tested successfully.
k) New production of the PDFE completed with early delivery of the samples. Preliminary functional tests are positive.
l) Digital board flight PCB delivered.

## 4.3. *Design Updates*

## 4.4. *Outstanding Problems*

## 4.5. *New Problems*

## 4.6. *Top Risks*

## 4.7. *Problem/Failure Quick Look*

# 5. Caltech/JPL (SEP) Status

## 5.1. *Summary of Status*

Activities centered on detector development, electronics development, and flight and GSE software development.

## 5.2. *Major Accomplishments:*

Critical Milestones:

- There were no critical milestones for LET and SEP Central in April.

Detectors:

- Micron Semiconductor delivered prototype detectors for LET and HET as follows:

  6 L1 detectors made from thick/thin etched wafers
  6 L1 detectors made from 20-micron membrane wafers
  2* L2 detectors
  2 L3 detectors
  2 H1 detectors
  2 H3 detectors

  Notes:
  * L2 detectors chips were mounted upside-down (see March 2003 progress report) and are not usable as flight detectors but are useful for testing the electrical performance of these devices. Micron will be replacing these with detectors that are correctly mounted.

- The junction-surface wire bonds on the H1, H3, and L3 detectors were inspected and looked good. These detectors were shipped to GSFC for further testing.
- Wire bonds on the back (ohmic) side of the L1 detectors were also inspected. These are of particular interest because on the membrane-type L1 detectors these bonds must be made to the unsupported thin silicon membrane. Micron had developed a fixture to support the membrane during wire bonding, and these are the first detectors we received that had been wire bonded using that fixture. The wire bonds on both the silicon and the circuit-board mounts looked good.
- Because of Micron's concerns that mounting the L2 detectors with their junction side glued to the mounts could possibly lead to electrical problems with the detectors, it was decided to redesign the L2 mounts so that the detectors can be mounted with the ohmic surface facing the mount, as Micron normally does.
- Nearly all fixturing for testing detectors at Caltech has been completed.

Electronics:

- This month focus has been on testing the SEP Central Logic/MISC EM board and writing flight S/W for it. At this point the MISC Actel design has been stable for several weeks and includes all needed functions. (There is one known problem affecting serial booting from the IDPU that will be fixed soon.) The EM board has been checked out rather completely. The MISC can be boot either serially (in spite of

the problem mentioned above) or from EEPROM. EEPROM has been loaded with the basic FORTH operating system. S/W development is proceeding with about 85% of code completed and tested. Tested functions include: generation of frame sync signals and distribution to LET, HET, and SIT, collection of science data from LET, HET, and SIT, ASCII command and command response flow through to LET, HET, and SIT, binary uploads to SEP, LET, HET, and SIT, sending of science, housekeeping, beacon, and command response packets to the IDPU simulator, the monitoring of the watchdog timer, reception and handling of the timing signals from the IDPU, and in-situ programming of the EEPROM. During S/W testing all instrument and IDPU real-time interactions are simulated using two separate GSE computers, one for the IDPU and one for the instruments. S/W functionality yet to be implemented includes booting the instruments and SEPT operation.

- The commanding document is being updated as we proceed.
- SEP Analog/Post-Reg EM board is in assembly/test at Space Instruments. Delay in MDM connector adapter delivery had slowed down the work, but the testing is now in full swing.
- SEP Bias Supply rigid-flex board fabricated by Pioneer Circuits. It is a flight-like EM board designed by Space Instruments and is now undergoing assembly and test by the same subcontractor.
- LET rigid-flex board layout finished and the board will be fabricated in early May. Due to the board's complexity, Protel auto-router was not able to handle it, so most of the routing had to be done by hand.
- EM parts kitted and shipped for Analog/Post-Reg, Bias Supply, second SEP Logic, and two HET boards.
- Started preliminary work on SEP external EM harness fabrication at JPL.
- Flight clock oscillator ordered from Q-Tech with BS screening level, in accordance with Project's Level 2 requirements.

Software:

- Worked on software development for SEP sensor simulator.
- Worked on LET onboard data processing algorithms.
- Worked on PHASIC testing software.
- Updated SEP Commanding/User Manual.

GSE:

- Modified GSE software to reflect recent format modifications.
- Worked with the SEP system engineer in testing the IDPU interface of the SEP logic board (ETU) using the IDPU simulator. Some initial problems were found with the IDPU simulator, but these have been worked around. The GSE is now accurately capturing the dummy telemetry messages being generated on the SEP logic board and sent over the IDPU interface. The GSE is now also able to send commands and dummy data uploads across the IDPU interface.
- Started work on software to support the IMPACT/SEP ETU Interface scheduled for May.

### 5.3. *Design Updates*

- Resource updates will be sent separately.

### 5.4. *Outstanding Problems*

- None

### 5.5. *New Problems*

- None.

### 5.6. *Top Risks.*

- The budget is very tight with no reserve being held at Caltech.
- Schedule slack that we show explicitly will be taken away from us.
- Development of the L1 detector. Risk mitigated by creating slack in schedule and by deciding to use more conventional manufacturing technique (Plan B detectors).

### 5.7. *Problem/Failure Quick Look*

- None.

# 6. SIT MONTHLY TECHNICAL PROGRESS REPORT

## 6.1. *SUMMARY of STATUS*

a. SIT TELESCOPE - Prototype is in house and working. Flight solid state detectors are in house, awaiting test. Flight Microchannel plates are in house and testing has begun.
b. SIT TOF System - FM1 has been downgraded to ETU and returned to UMd. Work is proceeding at MPAe to generate a new FM1 and FM2.
c. SIT Energy/Logic System - Prototype energy system has been integrated with the prototype TOF system and is functioning at UMd. ETU energy system is completed and under test. Front-end logic has been implemented at GSFC and is under test at UMd
d. SIT HVPS - HVPS ETU is being refurbished at UCB.

### 6.1.1. Schedule Changes

The current SIT schedule is available from David Rowse

## 6.2. *MAJOR ACCOMPLISHMENTS*

### 6.2.1. This Month

- Energy: Flight PCB fabrication completed and coupons submitted for inspection by GSFC.
- TOF: Alpha testing confirms ETU TOF and Energy meet science requirements for the flight system.
- Logic: Timing problems found in front-end logic and corrected in a third version of the Actel. Testing on this new unit was begun and so far has produced good results. Based on this we have begun design of the ETU logic board, including Actel with front-end logic and MISC, memory, SEP Central interface circuits, test points and first cut at housekeeping.
- Detectors: MCP testing continued

### 6.2.2. Next Month

We intend in May to complete ETU logic board design and PCB fabrication and hope to begin assembly of flight energy boards.

## 6.3. *DESIGN UPDATES*

### 6.3.1. Resources

| | Last Month | This Month | Change |
|---|---|---|---|
| Mass (kg) * | 1.46 | 1.46 | 0 |
| Power (mW) | 1.36 | 1.36 | 0 |
| Telemetry (bps) | 418 | 418 | 0 |

* Includes 200g book-kept by GSFC for SIT structure

### 6.4. *OUTSTANDING PROBLEMS*

We are continuing to work TOF parts issues.

### 6.5. *NEW PROBLEMS*

### 6.6. *NEW RISKS*

### 6.7. *PROBLEM/FAILURE QUICK LOOK*

Starts at first turn-on of flight hardware.

| ID # | Description | Assignee | Opened | Closed |
|---|---|---|---|---|
| | | | | |
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# 7. CESR (SWEA) Status

**CESR- TOULOUSE- France** **Author : Claude Aoustin / Project Manager**

## SWEA PROGRESS REPORT # 19
## (May 14, 2003)

## April 2003

CESR is in charge of :
- Electrostatic analyzer with deflectors, grids and Retractable Cover
- Detector consisting of two MCP rings
- Amplifiers and discriminators
- 3 High voltages

### 7.1. *Summary of Status*

#### 7.1.1. ETU1

Delivery to UCB was planned for 12/07/2002 : done 26/09/2002

#### 7.1.2. ETU2

Mechanical fabrication 100 % done
Integration done for the vacuum test configuration.
Electronic boards tested (100 %).

#### 7.1.3. FM1 / FM2

Mechanical fabrication 90 % done.
Surface treatment of the analyzer spheres done.
Surface treatment (gold, alodine) done.
Pin Puller integrated and tested.
Electronics boards fabrication :
Done for HV coupling board
Done for amplifiers board
Done for the HV board

### 7.2. *Major accomplishments*

Mechanical fabrication close to be completed.
HV coupling and amplifiers board populated : to be tested.
HV board : all components received – under population

### 7.3. *Design Updates*

Mass : 1040 g (EM is 950g without cover opening mechanism)
Power : 446 mW min ; 662 mW max

### 7.4. *Outstanding Problems*

Answer to comments on parts list sent.

Answer to comments on materials list sent. Waiting for the address where to sent the samples of Delrin and EP851.

Additional heater (0.5 watts) requested by the project. Location to be defined.

### 7.5. *New problems*

None

### 7.6. *Top Risks*

### 7.7. *Problem Failure Quick Look*

None

## 8. GSFC (MAG) Status

1. DPA for selected MAG parts was completed - all acceptable
2. MAG parts screening boards were designed and fab. Will proceed with parts screening immediately.
3. Magnetics characterization software has been completed.
4. Heater board design has been finalized. Zener diodes added for protection for worst case maximum bus voltage. MAG board re-layout is 98% complete
5. Continued to work SECHI and other magnetics issues

## 9. EPO at UCB

Monthly E/PO Report
April, 2003

**Formal Education:**

We have continued work on our magnetism and STEREO/IMPACT boom lesson. The major activities have been worked out and now we are beginning work on a teachers guide for the activities.

An abstract was submitted for a short course at the 2004 conference of the National Science Teachers Association (NSTA). The course will focus on the theme of the Sun-Earth connection.

Teacher professional development workshops on the Sun-Earth Connection were accepted for the October 2003 meeting of the Society for the Advancement of Chicanos and Native Americans in Science (SACNAS).

STEREO/IMPACT E/PO team is participating in a study group with other education professionals to learn better practices in curriculum development. In April we began to examine the concept of "Backward Design" advocated in the book *Understanding by Design*, by Wiggins and McTighe. This will help us learn to develop better STEREO/IMPACT education materials.

**Informal Education:**

N.Craig gave a talk at the E/PO session of the EGS/AGU/EUG Joint Assembly held in Nice, France, April 6-11, 2003. The Session was titled "Sharing the Geophysical Sciences with the Public at Science Centers, Museums, and Planetaria." The talk was titled the "Sounds of the Space- Listening to the Sun Earth Connection." This is a project that we are planning for the STEREO mission during the next years. The talk highlighted our "STEREO sounds" website and its future development as well as our plans for a museum kiosk for STEREO featuring imagery and sounds.

**Public Outreach:**

On April 12th, B. Mendez, and L. Peticolas participated in Cal Day on the campus of UC Berkeley. We presented E/PO materials from all our programs, gave tours of SSL, and gave public lectures about the some of the NASA missions at SSL, including STEREO.

SECEF E/PO Lead Community East-West Cost Meeting: N.C, B.J.M, and L.P attended this one day meeting in Baltimore at the Maryland Science Center. We heard about GSFC's Data Visualization Center and their desire to develop a greater variety of scientific visualizations for the space science community. We are investigating how STEREO related Modeling of the CMEs could be included in their portfolio.

"News and Events" 2003 STEREO/IMPACT web page updated.

Respectfully Submitted,
STEREO/IMPACT E/PO scientists Nahide Craig, Bryan Méndez, and Laura Peticolas