Lillian Reichenthal , Code 463.0
STEREO IMPACT Instrument Manager
Goddard Space Flight Center
Greenbelt, MD. 20771

Subject: IMPACT Monthly Technical Progress Report, Contract NAS5-00133

Lil:

Enclosed is the monthly technical progress report for the STEREO IMPACT project for the month of March 2003.

Sincerely,

David Curtis
IMPACT Project Manager
University of California, Berkeley

CC:

Julie.A.Janus.1@gsfc.nasa.gov
Debra.G.Dusterwald.1@gsfc.nasa.gov
Lillian.S.Reichenthal@nasa.gov
IMPACT Team

1. IMPACT Overview

This report is presented in sections by institution. Section 1 is an IMPACT Project Manager / System Engineer's overview.

1.1. *Contracting / Funding*

Funding through ~June 2003 is in place. Because of pipe-line delays in the system through to the subcontractors (Caltech and UMd) it is important that IMPACT be funded somewhat in advance of expected spending. There is some concern over the pending financial services shutdown at GSFC. The UCB contract needs to be adequately funded to cover the gap, and the GSFC CoIs need to get their orders out in advance. Even with the best planning there will be unexpected needs during this interval that could threaten our schedule.

The IMPACT budget situation has been worked continuously this month. Both the FY03 and the cost to complete have been constrained, and some science descopes have been proposed (which do not include loss of an instrument) to fit within the funding available with adequate margins. We hope to get this resolved in April.

1.2. *Significant System-Level Accomplishments*

- Participated in second half of Observatory CDR
- Prepared for and participated in Ground System Review
- Held IMPACT boom peer review at UCB
- Participated in EMC and Contamination Control Committee and MAG workshop meetings
- Worked IMPACT budget issues

1.3. *System Design Updates*

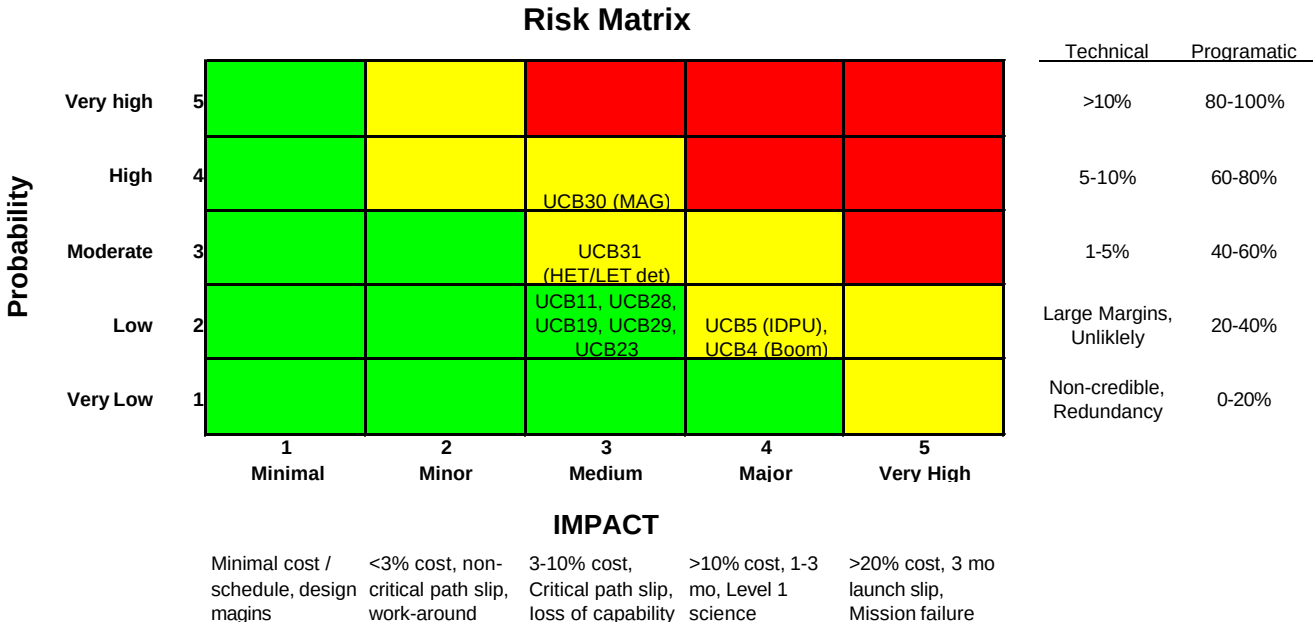
- None

1.4. *System Outstanding Issues*

- SEPT proton energy threshold not meeting requirement due to extra aluminum deposited to improve stray light rejection. Waiver submitted
- HET/LET detector adhesive material (outgassing) waiver submitted.

1.5. *Top 10 Risks*

Top 10 risks are attached. Note a reshuffling of risks and the addition of the SECCHI magnetics risk. Several risks have been mitigated to LOW.


Risk Matrix
Probability
Very high 5
High 4
Moderate 3
Low 2
Very Low 1
UCB30 (MAG)
UCB31 (HET/LET det)
UCB11, UCB28, UCB19, UCB29, UCB23
UCB5 (IDPU), UCB4 (Boom)
1 Minimal
2 Minor
3 Medium
4 Major
5 Very High
IMPACT
Technical
Programatic
>10%
80-100%
5-10%
60-80%
1-5%
40-60%
Large Margins, Unliklely
20-40%
Non-credible, Redundancy
0-20%
Minimal cost / schedule, design magins
<3% cost, non-critical path slip, work-around
3-10% cost, Critical path slip, loss of capability
>10% cost, 1-3 mo, Level 1 science
>20% cost, 3 mo launch slip, Mission failure

IMPACT Top Ten Risks 4/2003

No.	Risk Item	Score	Mitigation	Mitigation Schedule						
				PDR	EM Test	CDR	Sub-system Test	System Test	Env test	Early Orbit Test
UCB_5	IMPACT boom is a new design. Failure could affect Imager pointing requirements as well as boom-mounted instruments.	MEDIUM	Design for reliability. Early prototype testing. Adequate force margins.	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	LOW
UCB_30	SECCHI magnetics (especially filter wheen motor) may exceed magnetics requirement, impacting MAG science	MEDIUM	Screening test of ETU SECHHI parts ASAP. Evaluate possible screening or compensation techniques	MEDIUM	MEDIUM	MEDIUM	MEDIUM	LOW	LOW	LOW
UCB_4	The IDPU is a single point failure mechanisim for the IMPACT suite and PLASTIC	MEDIUM	IDPU is a simple, reliable system. Extra attention will be paid to ensuring its reliability, minimizing the risk of fault propagation. Early prototype testing; extensive FM testing	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM
UCB_31	HET/LET ETU detector mounting difficulties impacting schedule	MEDIUM	Idneticfy and solve problems; bring in outside experts to evaluate process, continue with flight detector fab in parallel	MEDIUM	MEDIUM	MEDIUM	MEDIUM	LOW	LOW	LOW
UCB_23	Non-standard parts qualification failure could impact delivery schedule	LOW	Early parts selection and screening	MEDIUM	MEDIUM	MEDIUM	LOW	LOW	LOW	LOW
UCB_27	Actel timing differences between flight & ETU parts may cause failures late in testing impacting delivery schedule	LOW	Do FM Thermal Vac early to allow time for finding and fixing timing problems; for designs on the critical path, consider installing a flight Actel in the ETU & thermal cycle.	MEDIUM	MEDIUM	MEDIUM	LOW	LOW	LOW	LOW
UCB_11	Stringent EMI requirements may delay schedule if testing fails	LOW	Careful design, ETU power converter testing, early system testing	MEDIUM	MEDIUM	MEDIUM	LOW	LOW	LOW	LOW
UCB_28	Thermal limitations of detectors result in a low bakeout temperature which might require a very long bakeout impacting delivery schedule	LOW	Bakeout subsystems prior to detector integration to reduce time of instrument-level bakeout; early bakeout	MEDIUM	MEDIUM	MEDIUM	LOW	LOW	LOW	LOW
UCB_19	Concern about fragility of ITO surfaces required to meet ESC requirements; failure will impact SWEA science	LOW	Replace ITO with more robust solution where possible; test ITO surfaces during I&T and replace when required	MEDIUM	MEDIUM	MEDIUM	LOW	LOW	LOW	LOW
UCB_29	LVPS behind schedule, on critical path; further slipping could delay delivery to spacecraft	LOW	Add manpower to LVPS task to avoid further slippage	MEDIUM	MEDIUM	MEDIUM	MEDIUM	LOW	LOW	LOW

2. Berkeley Status

2.1. *Summary of Status*

Schedule status through March to revised schedule has been provided separately.

2.2. *Major Accomplishments*

SWEA/STE:

- SWEA & SWEA/STE Interface ETU integration complete
- New SWEA/STE Interface DAC board layout complete
- New SWEA/STE Interface FPGA design complete, in analysis
- STE ETU detector mounts complete, ready to mount detectors
- Comparator screening problem resolved, part acceptable.

IDPU:

- Flight Software: IMPACT Build #2 complete except for a few bugs/features
- PLASTIC software Build #2.3 in progress, with a target delivery date of July for the IDPU/PLASTIC ETU interface test.

LVPS/HVPS:

- SIT HVPS re-layout complete.
- SWEA/STE LVPS layout complete
- PLASTIC LVPS layout complete
- SEP LVPS layout is ready to start
- IDPU LVPS efficiency worse than expected, resulting in some power increase. SEP & SWEA supplies still expected to meet targets.

Boom:

- First test samples from boom tubes have been delivered; some tweaks to process were required to smooth the slots that the rollers run in. Tubes are currently ~2weeks behind original schedule; we have not exceeded Qual unit contingency, and hope to make up some time in assembly.
- Protoflight machined parts in fab, also somewhat behind schedule, but compatible with the tube deliveries.
- Stacer on order, on schedule.
- Resolving pin puller sheer force margin improved by change in actuator (same electrical interface). Some small cost increase (~$5k), on schedule.
- Boom thermal-vac chamber long lead parts on order, remaining part orders soon.

GSE:

- SWEA/STE stand-alone GSE complete for instrument-level (no IDPU) tests.
- Decision taken to use IMPACT C&T GSE for PLASTIC. PLASTIC will still need science display GSE, but C&T GSE can serve as the PLASTIC POC, generating commands & displaying housekeeping.

2.3. *Design Updates*

- Change in boom deployment actuator to increase force.

2.4. *Outstanding Problems*

2.5. *New Problems*

2.6. *Top Risks.*

- Possible new ELDR testing requirement
- DAC screening failure puts SWEA/STE interface on boom suite critical path
- LVPS schedule tight

2.7. *Problem/Failure Quick Look*

None.

3. GSFC (SEP) Status

STEREO/IMPACT/SEP/GSFC Progress Report for March, 2003 – (von Rosenvinge, Baker, Hawk, Reames, Shuman, Wortman)

3.1. *Summary of Status*

Updated the GSFC SEP budget and schedule.

3.2. *Major Accomplishments*

- Produced outline drawings for the LET, Bias Supply, and the Low Voltage Power Supply.
- Completed HET electronics enclosure design.
- Completed layout of HET PC-board.
- Ordered 40 new L1 detector mounts.
- Revised thermal design after a review of the thermal blankets showed that ITO over GSFC Composite on Kapton is not viable.
- Reviewed Contamination Control in Solid-State Detector Lab with Therese Errigo.
- Worked on SEP commanding formats and other related issues.
- Decision made to revise L2 detector design so that ohmic side is not in contact with mount; Caltech to buy the new mounts.

3.2.1. Next Month-

- Revise L2 detector design.
- Update ICD with APL to include mounting hole diameters and correct LEMT FOV.
- Fabricate HET ETU electronics board.
- Complete LVPS and LET housing designs.
- Begin fabrication of various flight mechanical parts.
- Receive first detectors from Micron.
- Work on HET Particle Identification tables.

3.3. *Design Updates*

Need to update mass of SEP Main.

3.4. *Outstanding Problems*

We have still not received a contamination control plan from the Project. We also have not received approval of our waiver request for Shin-Etsu adhesive on the Micron detectors.

3.5. *New Problems*

The choice of thermal blanket materials is being revisited because of manufacturability problems.

3.6. *Top Risks*

No significant risks at GSFC? Need to ensure that manpower becomes available per the current plan.

3.7. ***Problem/Failure Quick Look***

4. Kiel/ESTEC (SEPT) Status

March 2003

4.1. *Summary of Status*

1. Fabrication of detector cables (subcontract to Axon Company) delayed due to misinterpretation of specifications. Clarification reached. No impact on flight model delivery in Nov. 2003.
2. Fabrication of door mechanism for EM delayed. Does not affect ETU interface test with SEP Central in June 2003.
3. PDFE programme according to schedule.
4. A YGT (Young Graduate Trainee) will help in testing and calibration of the Flight and Spare Model electronics as of June 2003.

4.2. *Major Accomplishments*

a) Fabrication of flight model housing started. Seven items (out of 30) complete.
b) Test of the first EM detector stack (out of 2) completed. One of the 6 diodes of this stack (2 central segments, 2 ring segments, 2 crosstalk segments) shows increased leakage current (20 nanoAmps instead of 5 nanoAmps) accompanied by increased noise (20 keV instead of 8 keV) in vacuum at ambient temperature.
c) Test of integrated EM detector/advanced breadboard electronics ongoing. No serious problem areas identified.
d) EM digital board delivered to ESTEC.
e) Design update of the FM/FS boards finished.
f) PDFE wafers for FM/FS produced.
g) Latchup tests completed in Louvain la Neuve accelerator (Belgium). Reports are being written but no concern expected.
h) Latchup board with decapsulated PDFE has been fully tested and is ready for test under californium source.
i) Initial tests on the EM digital board (which has a flight FPGA) shows a higher current consumption on the 2.6 V rail than was originally expected (32 mA average instead of 11 mA). New equivalent capacitors for the power consumption model were released by ACTEL (personal communication). The new estimation tends to confirm the measured value. Before to release any new figures, tests with the two boards (analog and digital) will be performed.
j) Updating of the "SEPT Operation Control and Data Processing Requirements" document ongoing. Minor changes are:
   - the single counter is now 24 bits instead of 23 bits deep,
   - the status word will have one more byte that contains the test generator pattern and amplitude which are used in the test generator mode.

4.3. *Design Updates*

4.4. *Outstanding Problems*

1. Common buy of thermal hardware (thermistor, thermostat, heater) still unclear (see SEPT Progress report November 2002).

4.5. *New Problems*

1. Increased power consumption (delta = +55 mW per FPGA, +110 mW per S/C) due to ACTEL flight FPGA (see 9. above).

4.6. *Top Risks*

4.7. *Problem/Failure Quick Look*

5. Caltech/JPL (SEP) Status

5.1. *Summary of Status*

Activities centered on detector development, electronics development, and flight and GSE software development.

Major Accomplishments:

Critical Milestones:

- Milestone 8 (LET-Place Flight Detector Order) of the IMPACT Critical Milestones chart dated 2/28/03 was accomplished. The order was initiated with Caltech purchasing in late February (see last month's report). Micron received the order on 5 March 2003.
- Milestone 4 (HET-Place Flight Detector Order) was accomplished on the same purchase order.

Detectors:

- Micron Semiconductor has assembled and wire-bonded detectors of all the designs needed for the HET and LET instruments including L1 detectors made both from etched thick/thin wafers and from 20-micron membrane wafers. The quantities of detectors assembled were as follows:

6	L1 detectors made from thick/thin-etched wafers
9[a]	L1 detectors made from 20-micron membrane wafers
3[b]	L2 detectors
4	L3 detectors
6	H1 detectors
6	H3 detectors

Notes:

a) Of the 9 membrane L1 detectors, 6 had good electrical characteristics before the vibration test. The other 3 were also vibrated since they can provide additional checks of survivability of the silicon chips and wire bonds in vibration.
b) L2 detectors chips mounted upside-down (see below).

- Vibration tests of these detectors were carried out on 20 March. All detectors survived the test and all wire bonds looked fine when inspected under a microscope after the test.
- In the process of assembling the detectors, a mistake was made in assembling the L2 detectors (50-micron thick detectors with 10 pads on the junction surface). The detector chips were glued into the mounts with the ohmic side in contact with the mount using Shin-Etsu silicone adhesive, as is Micron's normal practice, rather than with the junction surface in contact with the glue as intended. Micron proposed a way to modify the wiring of the detector to the mount that would allow us to do nearly all the normal testing of these prototype detectors' electrical response. We approved this approach and instructed Micron to continue with their plans to include the L2's in their testing.

- Micron received additional 20-micron wafers from Virginia Semiconductor. Starting from a batch of 35 thicker wafers, 3 were successfully lapped and polished to 20-micron thickness. Micron has now sent Virginia Semiconductor an additional 100 wafers (out of 350 that Micron purchased) for polishing to 20-microns. Micron also received the wafers intended for making 30-micron detectors, if that is required.

Electronics:

- The PHASIC hybrid test suite has been automated. A final run-through is needed before it is ready to test the flight hybrids.
- The design of the MISC Actel for SEP Central is underway. A design is up and running FORTH on our development board and all features except the IMPACT DPU interfaces have been checked. The only known problem in design is in serial boot operation (boot from prom is working). The cause of problem is known and the next version of the gate array should be ready for installation into the SEP Central EM logic board for further testing in early April.
- The SEP Central EM Logic board was fabricated by Pioneer Circuits and assembled at Caltech. This is a flight-like EM board with a few mounting holes that will need minor relocation in the flight layout. It is ready and waiting installation of the MISC Actel gate array. The EM unit PCB has rigid-flex pieces leading to Nanonics connectors. That aspect seems to have worked out well, with continuity verified from those connectors onto PCB.
- Early phases of SEP Central software development are proceeding in support of the development and test of the MISC Actel. The FORTH system has been adapted as needed and is up and running, including the power saving multi-tasker that utilizes clock gating.
- The SEP Analog/Post-Reg board was fabricated by Cirtech. It is a flight-like EM board designed by Space Instruments and will be assembled and tested by the same subcontractor.
- The SEP Bias Supply rigid-flex board was submitted to Pioneer Circuits for fabrication. It is a flight-like EM board designed by Space Instruments.
- The LET rigid-flex board is in the final stages of layout. It will be a flight-like EM board hosting PHASIC hybrids and the LET MISC.
- The latest intra-SEP ICDs were updated and issued.
- The PHASIC hybrid substrates were reworked at Teledyne and are now ready for the flight hybrid fab, which is in preparation and set to begin in early April at JPL.
- We obtained cost estimates for performing LET mock-up acoustic test and PHASIC hybrid thermal screening at the Environmental Test Lab at JPL. As an alternative to the latter, our own thermal chamber was reconfigured and tested. It was found to be capable of meeting the fail-safe requirements, so the 3-week hot soak required for each hybrid can now be conducted at Caltech with substantial savings.

Software:

- Worked on software development for the SEP sensor simulator.
- Worked on PHASIC testing software.
- Worked on definition of SEP command and command response formats.

GSE:

- Completed work on the software for extracting and displaying the fixed part of the SEP housekeeping packet in raw units (counts, ADC values, etc.). The software is based on the current description of the housekeeping packet.
- Completed work on the software for extracting and displaying SEPT Science packets in raw units based on the current packet description.
- Completed work on the software for extracting and displaying the non-event LET data in raw units based on the current packet descriptions.
- Started work on the software for logging data to the disk. The software is based on the current descriptions of the packets. As the packet description are finalized, some minor modifications of the above display software is expected. Also, additional displays will be added to cover the data in the currently undefined parts of the current packet descriptions and the LET events. Displays in engineering units will come after further hardware development.

5.2. *Design Updates*

- There were no resource changes for this month.

5.3. *Outstanding Problems*

- None

5.4. *New Problems*

- None.

5.5. *Top Risks.*

- The budget is very tight with no reserve being held at Caltech.
- Schedule slack that we show explicitly will be taken away from us.
- Development of the L1 detector. Risk mitigated by creating slack in schedule and by deciding to use more conventional manufacturing technique (Plan B detectors).

5.6. *Problem/Failure Quick Look*

- None.

6. SIT MONTHLY TECHNICAL PROGRESS REPORT

6.1. *SUMMARY of STATUS*

a. SIT TELESCOPE - Prototype is in house and working. Flight solid state detectors are in house, awaiting test. Flight Microchannel plates are in house and testing has begun.
b. SIT TOF System - FM1 has been downgraded to ETU and returned to UMd. Work is proceeding at MPAe to generate a new FM1 and FM2.
c. SIT Energy/Logic System - Prototype energy system has been integrated with the prototype TOF system and is functioning at UMd. ETU energy system is completed and under test. Front-end logic has been implemented at GSFC and is under test at UMd
d. SIT HVPS - HVPS ETU is being refurbished at UCB.

6.1.1. Schedule Changes

The current SIT schedule is available from Robert Palfy

6.2. *MAJOR ACCOMPLISHMENTS*

6.2.1. This Month

- Energy: Flight energy layout completed and ready for PCB fabrication.
- TOF: ETU testing begun with ETU energy and front-end logic.
- Logic: Race condition discovered in logic design and fixed. A new Actel has been created with the revised design and is under test. Wiring problem in test setup found and fixed. Software written for bench calibration.
- Detectors: MCP testing continued

6.2.2. Next Month

We intend in April to complete Logic testing , final logic board design and fabrication of flight energy board.

6.3. *DESIGN UPDATES*

6.3.1. Resources

	Last Month	This Month	Change
Mass (kg) *	1.46	1.46	0
Power (mW)	1.36	1.36	0
Telemetry (bps)	418	418	0

* Includes 200g bookkept by GSFC for SIT structure

6.4. *OUTSTANDING PROBLEMS*

We are continuing to work TOF parts issues.

6.5. *NEW PROBLEMS*

6.6. *NEW RISKS*

6.7. *PROBLEM/FAILURE QUICK LOOK*

Starts at first turn-on of flight hardware.

ID #	Description	Assignee	Opened	Closed

7. CESR (SWEA) Status

CESR- TOULOUSE- France **Author : Claude Aoustin / Project Manager**

SWEA PROGRESS REPORT # 18
(April 15, 2003)

March 2003

CESR is in charge of :
- Electrostatic analyzer with deflectors, grids and Retractable Cover
- Detector consisting of two MCP rings
- Amplifiers and discriminators
- 3 High voltages

7.1. *Summary of Status*

7.1.1. ETU1

- Delivery to UCB was planned for 12/07/2002 : done 26/09/2002

7.1.2. ETU2

- Mechanical fabrication 100 % done
- Integration done for the vacuum test configuration.
- Electronic boards tested (100 %).

7.1.3. FM1 / FM2

- Mechanical fabrication 80 % done.
- Surface treatment of the analyzer spheres done.
- Electronics boards fabrication :
    - Done for HV coupling board
    - Done for amplifiers board
    - Done for the HV board

7.2. *Major accomplishments*

- Mechanical fabrication close to be completed.
- HV coupling and amplifiers board under wiring.
- HV board : waiting for capacitors and resistors.

7.3. *Design Updates*

Mass : 1040 g (EM is 950g without cover opening mechanism)
Power : 446 mW min ; 662 mW max

7.4. *Outstanding Problems*

Answer to comments on parts list sent.

Answer to comments on materials list sent. Waiting for the address where to sent the samples of Delrin and EP851.

7.5. *New problems*

None

7.6. *Top Risks*

7.7. *Problem Failure Quick Look*

None

8. GSFC (MAG) Status

1. MAG board re-layout continues and is expected to be completed next week.
2. Several magnetic screening tests were completed including a scan of SECCHI mechanisms. Preliminary results predict a variable signature > 0.25 nT at the MAG sensor. Report in preparation but significant impact on test, integration and flight OPS expected. .
3. Test boards for parts screening have been laid out. However, the GSFC ban on procurements other than emergency is seriously impacting the completion of this effort.

9. EPO at UCB

Monthly E/PO Report
March, 2003

Formal Education:

Further development proceeded on our "Measuring Magnetism" lesson guide. Materials (such as magnets, compasses, iron filings, wires, batteries, and galvanometers) that a teacher would need for the lesson were purchased and the lessons were tested by the E/PO team. Demonstration pictures were taken for the lesson guide.

Informal Education:

A talk for the EGS-AGU-EUG Joint Assembly Meeting in Nice, France has been written entitled, "Sounds of Space: Listening to the Sun-Earth Connection." The talk highlights our "STEREO sounds" website and its future development as well as our plans for a museum kiosk for STEREO featuring imagery and sounds.

An abstract was submitted for a poster paper to given at the 202nd Meeting of the AAS entitled, "E/PO for STEREO/IMPACT and RHESSI missions."

Respectfully Submitted,
STEREO/IMPACT E/PO scientists Nahide Craig, Bryan Méndez, and Laura Peticolas