Lillian Reichenthal , Code 463.0
STEREO IMPACT Instrument Manager
Goddard Space Flight Center
Greenbelt, MD. 20771

Subject: IMPACT Monthly Technical Progress Report, Contract NAS5-00133

Lil:

Enclosed is the monthly technical progress report for the STEREO IMPACT project for the month of February 2003.

Sincerely,

David Curtis
IMPACT Project Manager
University of California, Berkeley

CC:

Julie.A.Janus.1@gsfc.nasa.gov
Debra.G.Dusterwald.1@gsfc.nasa.gov
Lillian.S.Reichenthal@nasa.gov
IMPACT Team

1. IMPACT Overview

This report is presented in sections by institution. Section 1 is an IMPACT Project Manager / System Engineer's overview.

1.1. *Contracting / Funding*

Funding through March 2003 is in place. Because of pipe-line delays in the system through to the subcontractors (Caltech and UMd) it is important that IMPACT be funded somewhat in advance of expected spending. There is some concern over the pending financial services shutdown at GSFC. The UCB contract needs to be adequately funded to cover the gap, and the GSFC CoIs need to get their orders out in advance. Even with the best planning there will be unexpected needs during this interval that could threaten our schedule.

Berkeley has provided a new budget to cover the effort at UCB. This budget includes all the incremental changes since the contract, including the recently recognized over-runs in parts caused by greater than anticipated screening and high rel parts costs, plus under-estimation of the boom tube costs. Details on these increases have been provided to Project. A Caltech budget update has also been sent in. GSFC work budgets have been re-worked with some unspent FY02 money from Mario Acuna's MAG effort going to cover the over-spending by the SEP effort at GSFC.

1.2. *Significant System-Level Accomplishments*

- Prepared for Observatory CDR
- Prepared for and participated in STEREO GPMC meeting
- Worked IMPACT budget issues
- Held MAG & SIT HVPS parts PCB. Discussed 50V ceramic capacitor issue
- PLASTIC programmer visited UNH to discuss requirement, interfaces, and PLASTIC simulator
- Decided we launch with survival heaters on.

1.3. *System Design Updates*

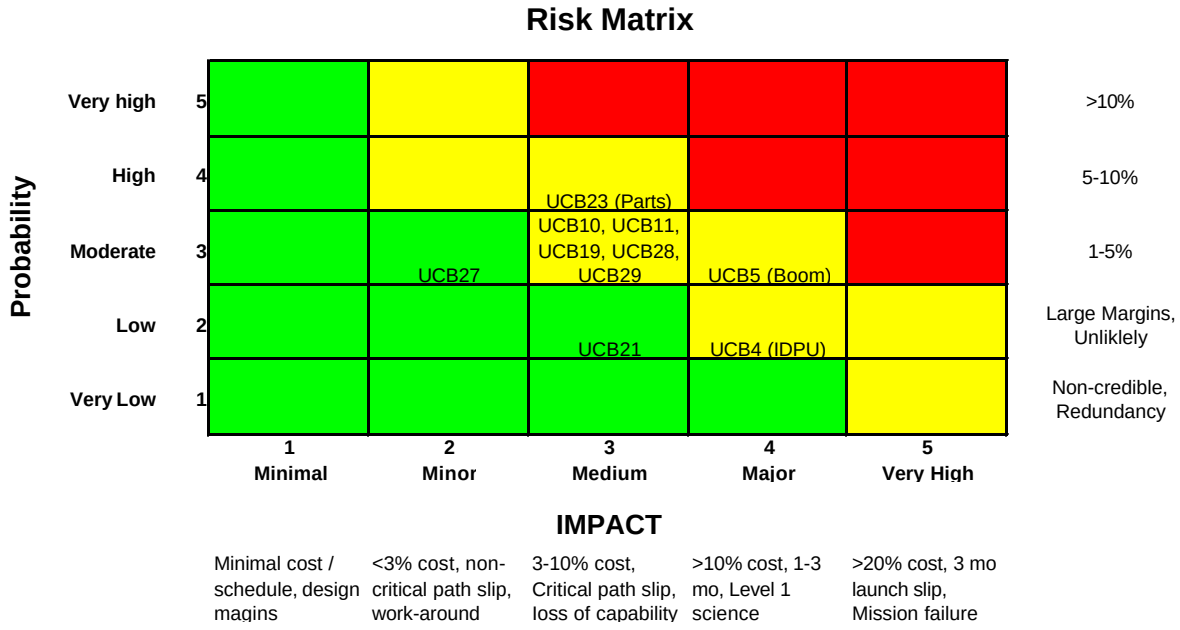
- None

1.4. *System Outstanding Issues*

- SEPT proton energy threshold not meeting requirement due to extra aluminum deposited to improve stray light rejection. Waiver submitted
- Need to decide if we launch with survival heaters on or off (currently on, trade between meeting thermal requirements and risk of launching powered on).

1.5. *Top 10 Risks*

Top 10 risks are attached. No change from last month.


Risk Matrix
Probability
Very high
5
High
4
Moderate
3
Low
2
Very Low
1
UCB23 (Parts)
UCB10, UCB11, UCB19, UCB28, UCB29
UCB27
UCB5 (Boom)
UCB21
UCB4 (IDPU)
>10%
5-10%
1-5%
Large Margins, Unliklely
Non-credible, Redundancy
1 Minimal
2 Minor
3 Medium
4 Major
5 Very High
IMPACT
Minimal cost / schedule, design magins
<3% cost, non-critical path slip, work-around
3-10% cost, Critical path slip, loss of capability
>10% cost, 1-3 mo, Level 1 science
>20% cost, 3 mo launch slip, Mission failure

IMPACT Top Ten Risks 1/2003

No.	Risk Item	Score	Mitigation	Mitigation Schedule						
				PDR	EM Test	CDR	Sub-system Test	System Test	Env test	Early Orbit Test
UCB_5	IMPACT boom is a new design. Failure could affect Imager pointing requirements as well as boom-mounted instruments.	MEDIUM	Design for reliability. Early prototype testing. Adequate force margins.	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	LOW
UCB_4	The IDPU is a single point failure mechanisim for the IMPACT suite and PLASTIC	MEDIUM	IDPU is a simple, reliable system. Extra attention will be paid to ensuring its reliability, minimizing the risk of fault propagation. Early prototype testing; extensive FM testing	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM
UCB_23	Non-standard parts qualification failure could impact delivery schedule	MEDIUM	Early parts selection and screening	MEDIUM	MEDIUM	MEDIUM	LOW	LOW	LOW	LOW
UCB_27	Actel timing differences between flight & ETU parts may cause failures late in testing impacting delivery schedule	MEDIUM	Do FM Thermal Vac early to allow time for finding and fixing timing problems; for designs on the critical path, consider installing a flight Actel in the ETU & thermal cycle.	MEDIUM	MEDIUM	MEDIUM	MEDIUM	LOW	LOW	LOW
UCB_11	Stringent EMI requirements may delay schedule if testing fails	MEDIUM	Careful design, ETU power converter testing, early system testing	MEDIUM	MEDIUM	MEDIUM	MEDIUM	LOW	LOW	LOW
UCB_28	Thermal limitations of detectors result in a low bakeout temperature which might require a very long bakeout impacting delivery schedule	MEDIUM	Bakeout subsystems prior to detector integration to reduce time of instrument-level bakeout; early bakeout	MEDIUM	MEDIUM	MEDIUM	MEDIUM	LOW	LOW	LOW
UCB_19	Concern about fragility of ITO surfaces required to meet ESC requirements; failure will impact SWEA science	MEDIUM	Replace ITO with more robust solution where possible; test ITO surfaces during I&T and replace when required	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	LOW
UCB_10	Complex Interlocking IMPACT schedule increases risk of late delivery to spacecraft	MEDIUM	Detailed fully integrated schedule developed and maintained with Project support. Monthly tracking of status.	MEDIUM	MEDIUM	MEDIUM	MEDIUM	LOW	LOW	LOW
UCB_29	LVPS behind schedule, on critical path; further slipping could delay delivery to spacecraft	MEDIUM	Add manpower to LVPS task to avoid further slippage	MEDIUM	MEDIUM	MEDIUM	LOW	LOW	LOW	LOW
UCB_18	LET Detectors from a new process	LOW	Backup L1 detectors; low risk, meet requirements; Continue parallel path with more robust 30 micron detectors at least to the wafer stage	MEDIUM	LOW	LOW	LOW	LOW	LOW	LOW

2. Berkeley Status

2.1. *Summary of Status*

Schedule status through February to revised schedule has been provided separately.

2.2. *Major Accomplishments*

SWEA/STE:

- SWEA/STE boards & FPGA in interface tests completed.
- Radiation test of replacement DACs completed, parts selected, procurement/screening of new DACs in progress
- New DAC board layout started, modifications to the controlling FPGA in progress
- Proton testing of ADC complete; part has been approved.
- Preparing STE detectors for mounting

IDPU:

- Flight Software: Build #2: SWEA code completed. Final details of Build 2 (outside of PLASTIC) are being ironed out, especially the PROM image.
- PLASTIC software Build #2 in progress.

LVPS/HVPS:

- IDPU LVPS completed, interface tested with IDPU. Some minor fixes to improve efficiency in progress.
- PLASTIC LVPS design modified to improve efficiency. Layout started
- SWEA LVPS layout ready to start
- SIT HVPS redesign near completion (temperature testing in progress), ready for final layout mods.

Boom:

- Almost all boom parts drawings completed review, have been quoted, going out to fab. This is somewhat behind schedule. A few final parts will be built in-house and are not on the critical path for the boom assembly.
- Resolving pin puller sheer force margin issue.
- Added force latch to gaurentee smallest boom segment deploys first (to provide extra margin for deployment of MAG harness)
- Added tray to control deployment of MAG harness
- FM Tube purchase order is out. Some delay due to materials at manufacturer (~1 week)
- Stacer on order
- Boom thermal-vac chamber is ready for quotes

GSE:

- Mag science module complete
- Some upgrades performed to IDPU C&T GSE

2.3. *Design Updates*

- Changes to accommodate a new DAC in SWEA/STE
- Small changes to boom design (see above)

2.4. *Outstanding Problems*

2.5. *New Problems*

Possible problem with comparator final screening tests (seems to have failed technology characterization). Analysis in work. If this part cannot be used, some candidate replacement parts have been identified, but board layouts would be affected (mostly on the SWEA/STE board which is already in re-layout for the DAC issue).

2.6. *Top Risks.*

Possible new ELDR testing requirement
DAC screening failure puts SWEA/STE interface on boom suite critical path
LVPS schedule tight
Comparator screening failure could impact flight build.

2.7. *Problem/Failure Quick Look*

None.

3. GSFC (SEP) Status

STEREO/IMPACT/SEP/GSFC Progress Report for February, 2003 – (von Rosenvinge, Baker, Hawk, Reames, Shuman, Wortman)

3.1. *Summary of Status*

- A significant number of detector mounts of each detector type were sent to Micron. Problems regarding wirebonding that Micron previously reported have apparently been resolved.
- Refined designs for SEP Main instrument box and internal components.
- Produced outline drawings for the Analog/Post-Regulator board and the Logic board for the SEP Main Assembly.
- Determined length of flexible strips needed to assemble the Flex-Rigid PCB's.
- Updated sizes for the HET Electronics and created outline drawing for HET Electronics board.
- Updated the GSFC SEP budget.

3.2. *Major Accomplishments*

3.2.1. Next Month-

- Complete all the PC-board outline drawings.
- Begin fabrication of various flight mechanical parts.
- Prepare for receipt of first detectors from Micron.
- Work on HET Particle Identification tables.
- Report test results of outgassing test on Shin-Etsu adhesive

3.3. *Design Updates*

Need to verify estimated mass impact of changes to SEP Main resulting from the design changes discussed above.

3.4. *Outstanding Problems*

- Problems and progress with detector mounts were discussed above.
- We have still not received a contamination control plan from the Project. We are unsure of the impact of this plan in terms of cost.

3.5. *New Problems*

The choice of thermal blanket materials is being revisited because of manufacturability problems.

3.6. *Top Risks*

No significant risks at GSFC? Need to ensure that manpower becomes available per the current plan.

3.7. *Problem/Failure Quick Look*

4. Kiel/ESTEC (SEPT) Status

February 2003

4.1. *Summary of Status*

1. No objections received in response to last month's re-baseline effort, hence we work with the new schedule.
2. Update of the flight board layout has started.

4.2. *Major Accomplishments*

a) Final report on the analysis of the door deployment mechanism received.
b) Final report on the structural analysis (FEM analysis) expected for March 2003.
c) Sensor housing for Engineering Model (EM) fabricated except for door mechanism. Final batch of pinpullers received.
d) Fit check of the coax harness completed. Fabrication of coax harness (6*13=78 coax cables) started. These are needed for final assembly of detector stacks for EM, FM, and FS.
e) Incoming inspection of EM detector stack performed. Vacuum tests are ongoing with commercial electronics and with the advanced breadboard of the analogue and digital electronics from ESTEC.
f) PDFE contract on its way. Burn in and test board defined by the manufacturer.
g) RAM for EM delivered. All remaining parts (resistors, capacitors) have been ordered.
h) Manufacturing of the EM boards started.
i) FPGA intermediate flight model delivered. It is a flight part which will be used to evaluate ground bounce problems. The part is burnt at FMI (Finland) and will be used for the EM.
j) Latchup mitigation technique test board manufactured (full digital board + one half analog board). One PDFE is decapsulated and will be placed under californium source.
k) TID tests finished. All parts meet the requirements.
l) Commercial parts (TLC2262, ADG704, ADG713, MAX892) are being decapsulated for individual LU testing foreseen in March (Louvain la Neuve, Belgium).
m) Flight mode operational sequences are being tested and refined.
n) SEPT Operation Control and Data processing requirements (V. 2.1) updated.
o) Functional tests of the advanced breadboard confirm the successful use of the clock signal provided by the FPGA to the PDFE, eliminating the need for a crystal. Hence the crystal procurement problem is closed.

4.3. **Design Updates**

4.4. **Outstanding Problems**

4.5. **New Problems**

4.6. **Top Risks**

4.7. **Problem/Failure Quick Look**

5. Caltech/JPL (SEP) Status

5.1. *Summary of Status*

Activities centered on detector development, electronics development, and flight and GSE software development.

Major Accomplishments:

Detectors:

- Micron Semiconductor ordered and received the new mask set for fabrication of L1 detectors on 3-inch diameter, lapped, and polished silicon wafers of 20-micron thickness. They started the processing of a number of wafers using this mask set. Completion of the first of these "Plan B" membrane L1 detectors is expected near the end of March.
- Micron ordered a set of 3-inch diameter silicon wafers from Wacher Siltronic (Germany). These will be sent to Virginia Semiconductor to be lapped and polished to a thickness of 30 microns, so that material of this thickness will be available should problems be encountered with the fabrication of the 20-micron L1 detectors.
- Purchase requisitions for all of the HET and LET flight detectors have been placed, and initial sets of mounts for all detector types were delivered to Micron. Micron began assembly of H1, H3, L2, and L3 detectors, and expects to have the prototype quantities completed and ready for environmental testing during the third week in March.
- Micron investigated the problems they had been having with wire bonds and found that they could obtain the required bond strengths using the preferred Si + 1% Mg wire by making the necessary adjustments to the wire bonding machine and by assuring that the operator had the necessary training and supervision. In addition, Micron made a wire-bonding jig to support the 20-micron L1 detectors during wire bonding. The first opportunity to see how well this wire bonding can be done will be in mid-March when the first membrane L1 detectors will be assembled and ready for wire bonding.

Electronics:

- PHASIC hybrid CDR/MRR (Critical Design Review/Manufacturing Readiness Review) was held at JPL and we were given the green light for flight hybrid fabrication. There was a problem with gold layer peeling from the hybrid substrate; it has been resolved by selective re-deposition of gold.
- Hybrid test algorithms are now complete and are being more fully automated by Andrew Davis.
- The issue of hybrid threshold variation has been addressed. During testing the threshold variation will be measured. Threshold margin against noise counting will be measured to allow optimum selection of threshold setting components, which will 1) compensate for threshold variation with temperature and 2) maintain a known acceptable margin of threshold above the noise floor over the entire temperature range. Each hybrid will be tested at -35, -15, 5, 25 and 45 C. The accommodation of the threshold variation has been studied and a conservative plan, which achieves all science requirements, is in place.

- SEP Logic rigid-flex board was submitted to Pioneer Circuits for fabrication. This is a flight-like EM board that hosts SEP Central MISC. Two identical EM boards will be assembled. The second unit will be used at GSFC as a SEP Central simulator for software development. The boards are expected back on 15 March 2003.
- Design of the MISC Actel gate array for the SEP Central logic board is in progress.
- Layout is proceeding on the LET front-end/logic rigid-flex board.
- The schematics for Analog/Post-Reg and Bias Supply boards were updated to include the latest procured parts and packaging information.
- Layout of the Analog/Post-Reg board was completed and it is now in final check.
- Progress was made on commanding issues, including the method of uploading binary data to our instruments.
- JPL safety and QA personnel performed a safety survey of the Caltech I&T facility and thermal burn-in chamber. A list of action items reflected the status of the facility and the need for improvements in several areas.
- JPL contamination control personnel performed a hydrocarbon survey of the Caltech I&T facility and found no obvious problems. In the meantime we've secured a class 1000 clean room for flight hardware I&T ("Galex Clean Room") which is superior to our current I&T facility (Room 5 Downs). The Downs facility will be used for EM I&T.

Software:

- Worked on software development for SEP instrument simulator.
- Worked on PHASIC testing software.
- Began definition of SEP command and command response formats.

GSE:

- Continued work on the SEP commanding software. Last month, there was a problem sending command directives to the IDPU simulator via the TCP/IP interface provided by the UCB STGSE software. After installing several new versions of the STGSE software, the problem persisted. To get around the problem, the commanding software was modified to no longer send to the STGSE software the directives that control sending commands; instead, the directives are now written to a script file, and the STGSE software executes them from the script file. The STGSE event log indicates that the directives are now being executed without a problem.
- Started work on the extraction and display of the fixed part of the SEP housekeeping packet. The software that extracts the housekeeping data from the TCP/IP packets has been written but not tested. The display software has not been started. The current effort is limited to displaying items in raw units.

5.2. *Design Updates*

- There were no resource changes for this month.

5.3. *Outstanding Problems*

- None

5.4. *New Problems*

- None.

5.5. *Top Risks.*

- The budget is very tight with no reserve being held at Caltech.
- Schedule slack that we show explicitly will be taken away from us.
- Development of the L1 detector. Risk mitigated by creating slack in schedule and by deciding to use more conventional manufacturing technique (Plan B detectors).

5.6. *Problem/Failure Quick Look*

- None.

6. SIT MONTHLY TECHNICAL PROGRESS REPORT
February 2003

6.1. *SUMMARY of STATUS*

a. SIT TELESCOPE - Prototype is in house and working. Flight solid state detectors are in house, awaiting test. Flight Microchannel plates are in house and testing has begun.

b. SIT TOF System - FM1 has been downgraded to ETU and returned to UMd. Work is proceeding at MPAe to generate a new FM1 and FM2.

c. SIT Energy/Logic System - Prototype energy system has been integrated with the prototype TOF system and is functioning at UMd. ETU energy system is completed and under test. Front-end logic has been implemented at GSFC and is under test at UMd

d. SIT HVPS - HVPS ETU is being refurbished at UCB.

6.1.1. Schedule Changes

The current SIT schedule is available from Robert Palfy

6.2. *MAJOR ACCOMPLISHMENTS*

6.2.1. This Month

- TOF: Work continued to resolve parts issues. Cabling was begun to allow testing of the ETU.

- Logic: Most effort this month was put into testing and troubleshooting the front-end logic. Most functions have been verified as working per specification but an intermittent problem possibly caused by an internal race condition has been discovered in the front-end logic (not the MISC). We are working with George Winkert at GSFC to resolve the problem. As part of this effort, we have ordered an Actel "Silicon Explorer" device allowing us to see internal nodes in the Actel and have modified the logic test board to accommodate the device.

- HVPS : UCB continued to work on the HVPS design. It was resolved to change the HVPS sync signal back to 100kHz to allow the sync to be derived from the 32.0Mhz logic clock.

- Detectors: All 5 of the MCP sets have been received from Burle and have been physically inspected. An off-centered metalization pattern on one set of plates was determined to be within acceptable limits. Functional testing and characterization of the plates has begun and will continue for some time.

6.2.2. Next Month

We intend in March to complete Logic testing, final logic board design, and release of the flight Energy board for PCB fabrication.

6.3. *DESIGN UPDATES*

6.3.1. Resources

	Last Month	This Month	Change
Mass (kg) *	1.46	1.46	0
Power (mW)	1.36	1.36	0
Telemetry (bps)	418	418	0

* Includes 200g bookkept by GSFC for SIT structure

6.4. *OUTSTANDING PROBLEMS*

We are continuing to work TOF parts issues.

6.5. *NEW PROBLEMS*

An intermittent problem in the front-end logic - probably a race condition - has been found and is being evaluated.

6.6. *NEW RISKS*

6.7. *PROBLEM/FAILURE QUICK LOOK*

Starts at first turn-on of flight hardware.

ID #	Description	Assignee	Opened	Closed

7. CESR (SWEA) Status

CESR- TOULOUSE- France **Author : Claude Aoustin / Project Manager**

SWEA PROGRESS REPORT # 17
(March 07, 2003)

February 2003

CESR is in charge of:

- Electrostatic analyzer with deflectors, grids and Retractable Cover
- Detector consisting of two MCP rings
- Amplifiers and discriminators
- 3 High voltages

7.1. *Summary of Status*

7.1.1. ETU1

Delivery to UCB was planned for 12/07/2002: done 26/09/2002

7.1.2. ETU2

- Mechanical fabrication 100 % done
- Integration done for the vacuum test configuration.
- Electronic boards tested (100 %).

7.1.3. FM1 / FM2

- Mechanical fabrication started (housing and spheres).
- Electronics boards fabrication:
    - Done for HV coupling board
    - Done for amplifiers board
    - On the way for HV board (green light received from UCB)

7.2. *Major accomplishments*

- Mechanical fabrication continues.
- Spheres have been sent to Switzerland for surface treatment (black copper).
- HV coupling board checked.
- Amplifiers boards under wiring.

7.3. *Design Updates*

Mass : 1040 g (EM is 950g without cover opening mechanism)
Power : 446 mW min ; 662 mW max

7.4. *Outstanding Problems*

- Answer to comments on parts list sent.
- Answer to comments on materials list sent. Waiting for the address where to sent the samples of Delrin and EP851.

7.5. *New problems*

None

7.6. *Top Risks*

7.7. *Problem Failure Quick Look*

None

8. GSFC (MAG) Status

Nothing to report.

9. EPO at UCB

Monthly E/PO Report

January, 2003

Formal Education:

> A draft was developed for a web-based curriculum piece on magnetism tying into the STEREO/IMPACT boom. The lesson has been developed for middle and high school students and will include tutorials for both teachers and students.

Respectfully Submitted,

STEREO/IMPACT E/PO scientists Nahide Craig and Bryan Méndez

February, 2003

Formal Education:

> Further development has proceeded for "Measuring Magnetism" a web-based curriculum piece on magnetism tying into the STEREO/IMPACT boom. The lesson has been developed to be flexible so that it might be used in either middle or high school. In the middle school portion students explore magnetism and discover that electronic equipment generates magnetic fields. In the high school portions students discover the connection between electricity and magnetism and eventually learn of the origin of magnetic fields.

We would also like to announce the addition of a new scientist to our E/PO team, Dr. Laura Peticolas. Laura will be spending one day per week working with us; she is a postdoc and has been working here at SSL on the FAST satellite. She is quite enthusiastic about education and adds the expertise of a space physicist to our group.

Respectfully Submitted,

STEREO/IMPACT E/PO scientists Nahide Craig, Bryan Méndez, and Laura Peticolas