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Subject: IMPACT Monthly Technical Progress Report, Contract NAS5-00133

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Enclosed is the monthly technical progress report for the STEREO IMPACT project for the month of January 2003.

Sincerely,

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CC:

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IMPACT Team

1. IMPACT Overview

This report is presented in sections by institution. Section 1 is an IMPACT Project Manager / System Engineer's overview.

1.1. *Contracting / Funding*

Funding through Feb 2003 is in place. Because of pipe-line delays in the system through to the subcontractors (Caltech and UMd) it is important that IMPACT be funded somewhat in advance of expected spending. A large increment is needed in March to cover detector purchases at Caltech and Boom purchases at Berkeley.

Berkeley has provided a new budget to cover the effort at UCB. This budget includes all the incremental changes since the contract, including the recently recognized over-runs in parts caused by greater than anticipated screening and high rel parts costs, plus under-estimation of the boom tube costs. Details on these increases have been provided to Project. Not yet included is an update of the Caltech budget, expected by the end of February. When that is in we hope to negotiate a contract mod.

1.2. *Significant System-Level Accomplishments*

- Updated schedules preparing new baseline
- Started getting PLASTIC IDPU programmer up to speed
- Participated in EMC & contamination committee meetings
- Prepared presentation for the GPMC schedule meeting and participated in dry-run
- Held discussions with PLASTIC on LVPS requirements
- Reviewed and signed off on new Spacecraft /IMPACT ICD

1.3. *System Design Updates*

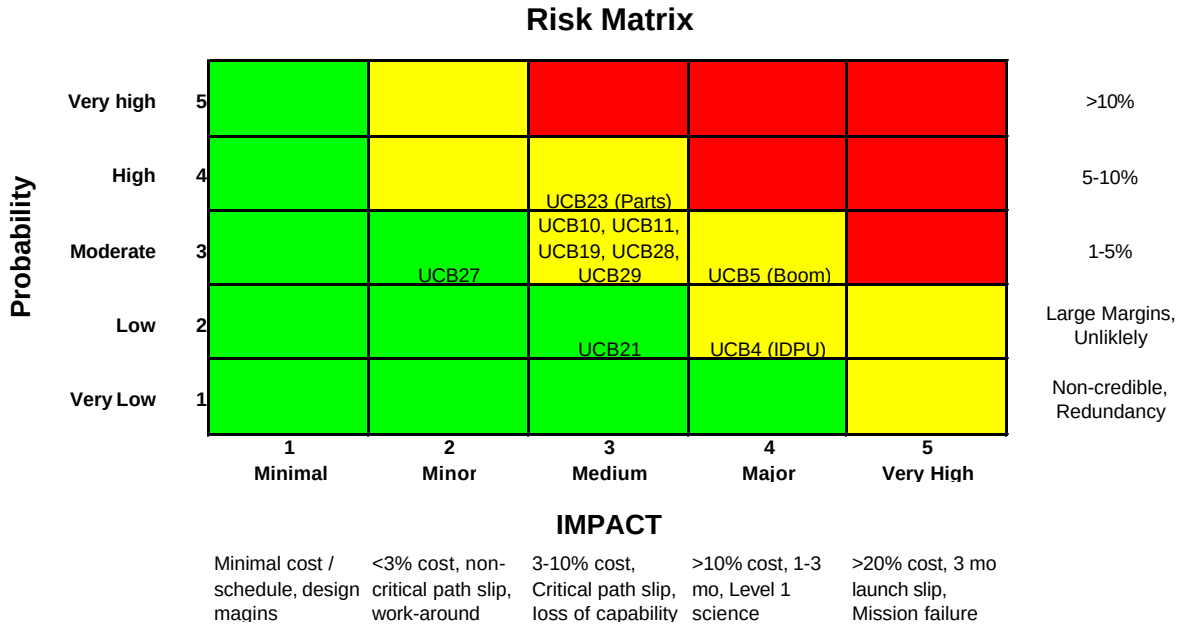
- None

1.4. *System Outstanding Issues*

- SEPT proton energy threshold not meeting requirement due to extra aluminum deposited to improve stray light rejection. Waiver submitted
- Need to decide if we launch with survival heaters on or off (currently on, trade between meeting thermal requirements and risk of launching powered on).

1.5. *Top 10 Risks*

Top 10 risks are attached. No change from last month.


Risk Matrix
Probability
Very high
5
High
4
Moderate
3
Low
2
Very Low
1
UCB23 (Parts)
UCB10, UCB11, UCB19, UCB28, UCB29
UCB27
UCB5 (Boom)
UCB21
UCB4 (IDPU)
>10%
5-10%
1-5%
Large Margins, Unliklely
Non-credible, Redundancy
1 Minimal
2 Minor
3 Medium
4 Major
5 Very High
IMPACT
Minimal cost / schedule, design magins
<3% cost, non-critical path slip, work-around
3-10% cost, Critical path slip, loss of capability
>10% cost, 1-3 mo, Level 1 science
>20% cost, 3 mo launch slip, Mission failure

IMPACT Top Ten Risks 1/2003

No.	Risk Item	Score	Mitigation	Mitigation Schedule						
				PDR	EM Test	CDR	Sub-system Test	System Test	Env test	Early Orbit Test
UCB_5	IMPACT boom is a new design. Failure could affect Imager pointing requirements as well as boom-mounted instruments.	MEDIUM	Design for reliability. Early prototype testing. Adequate force margins.	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	LOW
UCB_4	The IDPU is a single point failure mechanisim for the IMPACT suite and PLASTIC	MEDIUM	IDPU is a simple, reliable system. Extra attention will be paid to ensuring its reliability, minimizing the risk of fault propagation. Early prototype testing; extensive FM testing	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM
UCB_23	Non-standard parts qualification failure could impact delivery schedule	MEDIUM	Early parts selection and screening	MEDIUM	MEDIUM	MEDIUM	LOW	LOW	LOW	LOW
UCB_27	Actel timing differences between flight & ETU parts may cause failures late in testing impacting delivery schedule	MEDIUM	Do FM Thermal Vac early to allow time for finding and fixing timing problems; for designs on the critical path, consider installing a flight Actel in the ETU & thermal cycle.	MEDIUM	MEDIUM	MEDIUM	MEDIUM	LOW	LOW	LOW
UCB_11	Stringent EMI requirements may delay schedule if testing fails	MEDIUM	Careful design, ETU power converter testing, early system testing	MEDIUM	MEDIUM	MEDIUM	MEDIUM	LOW	LOW	LOW
UCB_28	Thermal limitations of detectors result in a low bakeout temperature which might require a very long bakeout impacting delivery schedule	MEDIUM	Bakeout subsystems prior to detector integration to reduce time of instrument-level bakeout; early bakeout	MEDIUM	MEDIUM	MEDIUM	MEDIUM	LOW	LOW	LOW
UCB_19	Concern about fragility of ITO surfaces required to meet ESC requirements; failure will impact SWEA science	MEDIUM	Replace ITO with more robust solution where possible; test ITO surfaces during I&T and replace when required	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	LOW
UCB_10	Complex Interlocking IMPACT schedule increases risk of late delivery to spacecraft	MEDIUM	Detailed fully integrated schedule developed and maintained with Project support. Monthly tracking of status.	MEDIUM	MEDIUM	MEDIUM	MEDIUM	LOW	LOW	LOW
UCB_29	LVPS behind schedule, on critical path; further slipping could delay delivery to spacecraft	MEDIUM	Add manpower to LVPS task to avoid further slippage	MEDIUM	MEDIUM	MEDIUM	LOW	LOW	LOW	LOW
UCB_18	LET Detectors from a new process	LOW	Backup L1 detectors; low risk, meet requirements; Continue parallel path with more robust 30 micron detectors at least to the wafer stage	MEDIUM	LOW	LOW	LOW	LOW	LOW	LOW

2. Berkeley Status

2.1. *Summary of Status*

Schedule status through Jan 31 to revised schedule has been provided separately.

2.2. *Major Accomplishments*

SWEA/STE:

- SWEA/STE boards & FPGA in interface tests.
- SWEA pedestal ETU box complete & fit-checked.
- Preparing for radiation test of replacement DACs
- STE door life tests up to 9,000 cycles without failure (expected on-orbit cycles = 300). Making a modification to reduce risk of actuator wire fouling. Vibration test pending.
- Preparing STE detectors for mounting

IDPU:

- Flight Software: Build #2: SWEA code in test

LVPS/HVPS:

- IDPU LVPS load/test in progress
- SIT HVPS in re-design to accommodate changed requirements, better synchonization over temperature
- Detailed designs for SWEA, SEP, and PLASTIC LVPS complete. Layout waiting for results from IDPU ETU tests.

Boom:

- Parts drawings are complete and reviewed. Resulting red-lines are in work. Parts will go out quote soon
- FM Tube purchase order is out, mandrel has been checked & delivered.
- Stacer on order
- Boom thermal-vac chamber is in detailed design.

GSE:

- Further APL emulator testing performed with new rev (better).
- MAG science module in progress

2.3. *Design Updates*

- Changes to accommodate a new DAC in SWEA/STE pending results of radiation tests

2.4. *Outstanding Problems*

- ADC SEL latent damage issue. SEL test performed, results look good but analysis not complete. Further testing may be required.

2.5. *New Problems*

2.6. *Top Risks.*

ADC Latent damage issue (see above).
Possible new ELDR testing requirement
DAC failure puts SWEA/STE interface on boom suite critical path
LVPS schedule tight

2.7. ***Problem/Failure Quick Look***

None.

3. GSFC (SEP) Status

STEREO/IMPACT/SEP/GSFC Progress Report for January, 2003 – (von Rosenvinge, Baker, Hawk, Reames, Shuman, Wortman)

3.1. *Summary of Status*

The GSFC schedule was reworked with Bob Palfy as part of the Project-wide schedule review. Some apparent problems were removed by restructuring the dependencies and/or need dates. The schedule is tight in some places but doable.

Detector mounts have now been received for all detector types and are in various stages of coupon testing, visual inspection, mechanical inspection and installation of connectors. Problems reported by Micron with wire-bonding to L1 detector mounts led to extensive tests on our part to identify the source of the problem. Micron had complained of "flakey gold" and an inability to make bonds without resorting to excessive bonding pressure. The latter caused the bonded pads to be too thin at the ankles, resulting in broken bond wires. We received 10 L1 mounts (made by Speedy Circuits) back from Micron. One of these was tested for Ni thickness, Au thickness, Au softness, and organic and inorganic contamination. None of these tests indicated anything wrong with this mount. We then made test bonds to several of these mounts, first with Al(1% Si) wire, and then with Al(1%Mg) wire which we received from Micron. These test bonds all passed pull-tests. In addition, sample L2 and L3 mounts (made by Rigiflex) were sent to Micron and Micron successfully bonded to them. Micron has small numbers of each mount type. Word as of this moment is that Micron has in fact succeeded in bonding to one of the original 10 mounts from Speedy Circuits. We will be shipping quite a few more mounts next month, assuming that the wire-bonding problems have been resolved at Micron.

The mechanical design of the SEP Main box has been revised to accommodate a larger low voltage power supply. This involved widening the footprint, which a vibration analysis just before CDR had indicated was also needed in order to not exceed the pull-strength of the inserts in the honeycomb panel to which the box is attached. The revised assembly mistakenly had LET oriented at 45 degrees (the mean Parker spiral angle) rather than 50 degrees, resulting in an inadvertent partial blocking of the LET field of view. Revised drawings for circuit-board layout have been completed except for the HET and LET telescopes. HET layout is near completion but is currently being held up until the required revisions are completed.

Software has been completed capable of setting up differential HET serial commands. Previously, the HET commanding setup a single 846-bit serial command register for one PHASIC chip. We can now setup 2 serial command registers, one for each PHASIC chip, and either change the overall command register contents or change only specific subsets of command bits.

Serial Command Interface Build 2 software and the Serial Command Interface User's Guide for Build 2 have both been completed.

3.2. *Major Accomplishments*

3.2.1. Next Month-

a Complete all the PC-board outline drawings.
b Begin fabrication of various flight mechanical parts.
c Prepare for receipt of first detectors from Micron.
d Work on HET Particle Identification tables.
e Review and revise the GSFC/SEP budget.

3.3. *Design Updates*

Need to verify estimated mass impact of changes to SEP Main resulting from the design changes discussed above.

3.4. *Outstanding Problems*

Problems and progress with detector mounts were discussed above.

We have still not received a contamination control plan from the Project. We are unsure of the impact of this plan in terms of cost.

3.5. *New Problems*

Increased costs will be quantified next month.

3.6. *Top Risks*

No significant risks at GSFC? Need to ensure that manpower becomes available per the current plan.

3.7. *Problem/Failure Quick*

4. Kiel/ESTEC (SEPT) Status

January 2003

4.1. *Summary of Status*

1. Contract signed with IMEC for PDFE ASIC. This removes uncertainty for FM schedule.
2. SEPT schedule re-baselined and submitted. Total slack: -17 days (FM1) and - 26 days (FM2). This slack will increase, if accelerator calibration is done prior to delivery (preferred), else SEPT needs to be returned for calibration in 2004 during time slot of end-to-end test. [Note that this negative slack is to the old schedule; we have positive slack to the new schedule completed in February].

4.2. *Major Accomplishments*

a) The analysis of the door deployment mechanism was completed, resulting in changes of some design details. Final report will be submitted in February 2003.
b) The SEPT structural analysis (FEM analysis) was completed. The primary structural vibration mode is 66.4 Hz (requirement: > 50 Hz). The margin of safety (MOS) on yield strength is 6.2 on bracket and 3.7 on S/C platform (requirement: >0). The MOS on ultimate strength is 7.4 on bracket and 4.1 on S/C platform (requirement >0). Final report will be submitted in February 2003.
c) Canberra has delivered the first (out of 15) completely assembled detector stacks. It will be integrated in the ETU (total of 2 stacks needed for ETU.) This is necessary for a fit check of the coax harness. Thereafter, the remaining 14 stacks can be assembled. Note: the previously delivered detectors were considered prototypes.
d) A second and improved breadboard of the analogue and digital electronics was completed at ESTEC and delivered from ESTEC to Kiel. It will be integrated with the ETU detector stack for tests and later replaced by the ETU electronics. The RAM for the ETU electronics is still to be delivered.
e) Completion of this advanced breadboard has allowed to measure weight and power more realistically. Some estimation is still necessary to predict the power consumption with flight components. The actual weight is 130 g (4 g heavier than CDR figures), the actual power estimation is 572 mW (79 mW higher than CDR figures). A detailed power rationale will be made available to Branislav.
f) Functional tests of the advanced breadboard show the successful use of the clock signal provided by the FPGA to the PDFE. If further tests confirm this feature, the crystal procurement problem is closed.

4.3. *Design Updates*

4.4. *Outstanding Problems*

4.5. *New Problems*

1. Power consumption increase by 16 % (see above item 5).

4.6. *Top Risks*

4.7. *Problem/Failure Quick Look*

5. Caltech/JPL (SEP) Status

5.1. *Summary of Status*

Activities centered on detector development, electronics development, and flight and GSE software development.

5.2. *Major Accomplishments:*

Detectors:

- A meeting was held with Micron Semiconductor's Managing Director and key design and production staff members on January 16-17 at Caltech.
- The decision was made to proceed with the fabrication of the flight L1 detectors using lapped and polished silicon wafers of 20-micron thickness and 3-inch diameter (plan B). In addition, it was decided that Micron Semiconductor should proceed with the fabrication of a new mask set for the production of these detectors. The existing mask set contains two copies of the L1 pattern, and the new mask set will double this number thereby improving the yield per wafer started into production. Micron has designed the new mask set and delivered a drawing for review. They also provided price quotations for the new mask set and the flight detector fabrication and testing. Purchase requisitions from Caltech were initiated for these items.
- Micron also provided quotations for fabrication of flight L1 detectors using 30-micron wafers, which could serve as a back up to the baseline 20-micron devices should we encounter problems with production yields or testing failures for the thin version. The quotation separately covers procurement and polishing of the wafers and the flight detector fabrication. An order for the wafer procurement and polishing was placed from Caltech so that the material will be available should we need to exercise the 30-micron fallback option.
- Micron has been investigating the problems that were encountered with the electrical contacts on prototype L1 and H3 detectors, with support from GSFC and JPL. On the biased side of L1 detectors, Micron had made contacts using conductive epoxy because they were having difficulty wire bonding to the 20-micron membrane. However, the conductive epoxy cracked and the contacts failed before the prototypes arrived at Caltech. Micron agrees that this was not an appropriate solution to the wire-bonding problem and had now developed a fixture, which will support the silicon membrane during wire bonding. There were also problems of failed wire bonds on the circuit-board mounts.
- Tests at GSFC indicated that the plating on the mounts is adequate and not contaminated. Part of the bonding problem has been traced to poor bonding technique by an inexperienced technician---Micron plans to have future wire bonding activities over-seen by an experienced production supervisor and to do more-formal QA inspections. Micron and GSFC are also looking at whether the use of Al + 1% Mg wire (which is planned to minimize the chance of wire bond failures cue to vibration and acoustics) may be responsible for some of the difficulty getting strong bonds to the mounts.
- Mounts for the H1, L2, and L3 detectors (made by Rigiflex) passed inspection at GSFC and are shipped to Micron..

Electronics:

- JPL assembled six more flight hybrids with PHASIC-2 die. Three out of seven hybrids have a good die, while the other four have imperfections on the die that have typically disabled 1-2 channels out of 32 channels per die.
- Preparations are under way for PHASIC hybrid CDR in early February.
- The I&T facility improved with the introduction of a high-pressure air line that enabled us to start temperature testing of PHASIC hybrids.
- A detailed study of hybrid performance and the development of a complete test suite are underway. All fixes that were installed to the die design and layout have been verified to work nominally. Only one change in hybrid design has resulted from detailed VLSI performance study: a resistor that sets the threshold for all peak detector discriminators has been removed from the hybrid and will be replaced with an external network consisting of two resistors and one thermistor. This allows optimal choice of threshold setting and temperature compensation separately for each hybrid. This change was needed due to a larger than expected variance in peak detector thresholds across the 32 ADCs on each VLSI chip.
- The DC test routines are defined and are being automated. The AC tests are still in development but are about 75% defined and 50% automated.
- The study of hybrid performance has moved to the stimulation of the circuitry using a "real" detector source: a NaI crystal viewed by a photomultiplier tube. High fidelity pulse height spectra have been obtained for a Cs137 gamma-ray source. Differential linearity is impressively good with no channel-to-channel width variation yet detected down to approximately the 1% level. In fact, by summing the counts in even and odd bins over a portion of the Cs137 spectrum which contains just a smooth continuum, the average difference in bin widths between even and odd bins was found to be less than 0.06%. The difference in summed counts was consistent with statistical variations and zero bin-width difference between even and odd bins. However, for bins just above threshold the continuum spectrum showed some irregularities. So the differential linearity was measured using a ramped test pulser, finding that for normal setting of the programmable AOG level just above the noise floor the first few bins above threshold are wider than nominal by about 5%, with the width decreasing monotonically to nominal within about 10 - 20 bins. However, at high AOG threshold settings there is a much more pronounced widening of the bins just above threshold, of as much as 50-70%. These results probably do not represent some malfunction, but rather are due to intentional (but perhaps excessive) high frequency filtering of the signal after the AOG stage which tends to make the peak height at the peak detector somewhat sensitive to the integrated area of the portion of the pulse passed by the AOG rather than just its peak amplitude. The rather small (5%) differential non-linearity obtained for low threshold settings cannot, however, account for the irregularity of the continuum spectrum obtained with the Cs137 source and so investigation continues, with rate and pile-up effects the next topic.
- Received preliminary PCB outlines with mounting hole locations for Bias Supply, Analog/Post-Reg and Logic boards. Part footprints have been finalized and layout has started on EM versions of these three boards.
- Ordered EM and flight Nanonics connectors from Tyco Electronics, and EM and flight SRAM 128k x 8, 3.3V from Honeywell.
- Decided to use distributed chip resistors for survival and operational heaters where needed on LET and SEP Central.

Software:

- Worked on hardware and software development for SEP instrument simulator.
- Worked on PHASIC testing software.
- Developed draft of SEP Housekeeping CCSDS packet.
- Developed draft of SEPT science CCSDS packets.

GSE:

- Completed the first version of the IDPU simulator adapter code. This code is designed to take the telemetry from the TCP/IP interface provided by UCB-furnished STGSE software which operates the IDPU simulator, convert the telemetry to payload telemetry packets, and fan it out to the rest of the SEP GSE software. In addition, it takes the SEP commands, generates the necessary directives (commands) for the simulator, and ships these to the STGSE software via the TCP/IP interface.
- Wrote a data generator as a stand-in for the STGSE software to test the telemetry conversion and fan out parts of the IDPU simulator adapter code. The adapter code successfully produces payload telemetry packets and fans out the telemetry for the other parts of the SEP GSE software using this stand-in data generator. (Once sufficient pieces of the SEP engineering model are complete, the stand-in data-generator will be removed, and the flow of telemetry from SEP thru the IDPU simulator and STGSE software will be tested.)
- Wrote the first version of the SEP commanding software. The only source of commands in this current version is the keyboard. Later versions will allow users to send disk-stored sets of commands.
- Started testing the entire commanding path from the SEP commanding software (third item above) to the adapter software (first item above) and thru the TCP/IP interface of the STGSE software, which forwards the commands to the IDPU simulator for SEP (if it was present). As of this writing, this has only been partially successful. The successful part is that the entire path works at very slow speeds. The unsuccessful part is that it ONLY works at very slow speed. The problem appears to be in the TCP/IP communications between the SEP GSE software and the STGSE software from UCB. The problem is currently being examined.

5.3. *Design Updates*

- Resource updates will be sent separately.

5.4. *Outstanding Problems*

- None

5.5. *New Problems*

- None.

5.6. *Top Risks.*

- The budget is very tight with no reserve being held at Caltech.
- Schedule slack that we show explicitly will be taken away from us.
- Development of the L1 detector. Risk mitigated by creating slack in schedule and by deciding to use more conventional manufacturing technique (Plan B detectors).

5.7. *Problem/Failure Quick Look*

- None.

6. SIT MONTHLY TECHNICAL PROGRESS REPORT
January 2002

6.1. *SUMMARY of STATUS*

a. SIT TELESCOPE - Prototype is in house and working. Flight solid state detectors are in house, awaiting test.
b. SIT TOF System - FM1 has been downgraded to ETU and returned to UMd. Work is proceeding at MPAe to generate a new FM1 and FM2.
c. SIT Energy/Logic System - Prototype energy system has been integrated with the prototype TOF system and is functioning at UMd. ETU energy system is completed and under test. Front-end logic has been implemented at GSFC and is under test at UMd
d. SIT HVPS - HVPS ETU has been returned to UCB for refurbishment.

6.1.1. Schedule Changes

The current SIT schedule is available from Robert Palfy

6.2. *MAJOR ACCOMPLISHMENTS*

6.2.1. This Month

a Energy Board: The ETU energy board assembly was completed and testing begun. Testing has proceeded to the point that we are convinced the circuit is working properly.
b TOF:
c Logic : The prototype PWB was received and has had the socket successfully attached. It awaits final assembly to allow testing of the front-end logic Actel chip.
d HVPS: Redesign continued at UCB. ETU life test continued at UMd. This test is proceeding with no problems noted in the behavior of the HVPS.

6.2.2. Next Month

In February we intend to finish assembly and test of the ETU energy board and to begin testing the front-end logic Actel. We need to begin testing on the solid state detectors. We expect to receive the flight micro-channel plates in January.

6.3. *DESIGN UPDATES*

6.3.1. Resources

	Last Month	This Month	Change
Mass (kg) *	1.46	1.46	0
Power (mW)**	1.36	1.36	0
Telemetry (bps)	418	418	0

* Includes 200g bookkept by GSFC for SIT structure
** Note: Mass and power increases due to measured values for ETU HVPS

6.4. *OUTSTANDING PROBLEMS*

6.5. *NEW PROBLEMS*

Inspection of the "Flight Unit 1" TOF boards at GSFC has uncovered a number of problems of varying severity. We need to evaluate these problems and identify changes needed to bring these and/or the following TOF boards to flyable status.

6.6. *RISKS*

6.7. *PROBLEM/FAILURE QUICK LOOK*

Starts at first turn-on of flight hardware.

ID #	Description	Assignee	Opened	Closed

7. CESR (SWEA) Status

CESR- TOULOUSE- France **Author : Claude Aoustin / Project Manager**

SWEA PROGRESS REPORT # 16
(February 12, 2003)

January 2003

CESR is in charge of :
- Electrostatic analyzer with deflectors, grids and Retractable Cover
- Detector consisting of two MCP rings
- Amplifiers and discriminators
- 3 High voltages

7.1. *Summary of Status*

7.1.1. ETU1

Delivery to UCB was planned for 12/07/2002 : done 26/09/2002

7.1.2. ETU2

Mechanical fabrication 100 % done
Integration done for the vacuum test configuration.
Electronic boards tested (100 %).

7.1.3. FM1 / FM2

Mechanical fabrication started (housing and spheres).
Electronics boards fabrication:
Done for HV coupling board
On the way for amplifiers board
Standby for HV board (waiting for integration test in UCB)

7.2. *Major accomplishments*

ETU2 fabrication
Mechanical fabrication:
Finished. Integration done in two parts for MCP test purpose (up to the MCP stack and internal sphere).
The upper part (external spheres – grids – deflectors and pin puller) is ready as well.
Electronics :
The 3 boards are tested and integrated in the box.

7.3. *Design Updates*

Mass : 1040 g (EM is 950g without cover opening mechanism)
Power : 446 mW min ; 662 mW max

7.4. *Outstanding Problems*

Answer to comments on parts list sent.

7.5. *New problems*

None

7.6. *Top Risks*

7.7. *Problem Failure Quick Look*

None

8. GSFC (MAG) Status

Nothing to report.

9. EPO at UCB

Monthly E/PO Report

Nothing to report.