Lillian Reichenthal , Code 463.0
STEREO IMPACT Instrument Manager
Goddard Space Flight Center
Greenbelt, MD. 20771

Subject: IMPACT Monthly Technical Progress Report, Contract NAS5-00133

Lil:

Enclosed is the monthly technical progress report for the STEREO IMPACT project for the month of December 2002.

Sincerely,

David Curtis
IMPACT Project Manager
University of California, Berkeley

CC:

Julie.A.Janus.1@gsfc.nasa.gov
Debra.G.Dusterwald.1@gsfc.nasa.gov
Lillian.S.Reichenthal@nasa.gov
IMPACT Team

1. IMPACT Overview

This report is presented in sections by institution. Section 1 is an IMPACT Project Manager / System Engineer's overview.

1.1. *Contracting / Funding*

Funding through Feb 2003 is in place. Because of pipe-line delays in the system through to the subcontractors (Caltech and UMd) it is important that IMPACT be funded somewhat in advance of expected spending.

There have been a significant number of items agreed upon between IMPACT and Project that involve incremental funding. We need to mod the contract to reflect those changes. The first step is to agree upon what those changes are, which is in progress.

Preliminary indications are that under-runs in some manpower loading (resulting in work behind schedule, notably the LVPS) is masking over-runs in EEE parts. More detail to follow.

1.2. *Significant System-Level Accomplishments*

- Updated boom and power converter schedules
- Worked on organizing parts lists for easier reference
- Held an IMPACT team meeting
- Generated recovery plan for DAC failure
- Measured "Broken Boom" stiffness

1.3. *System Design Updates*

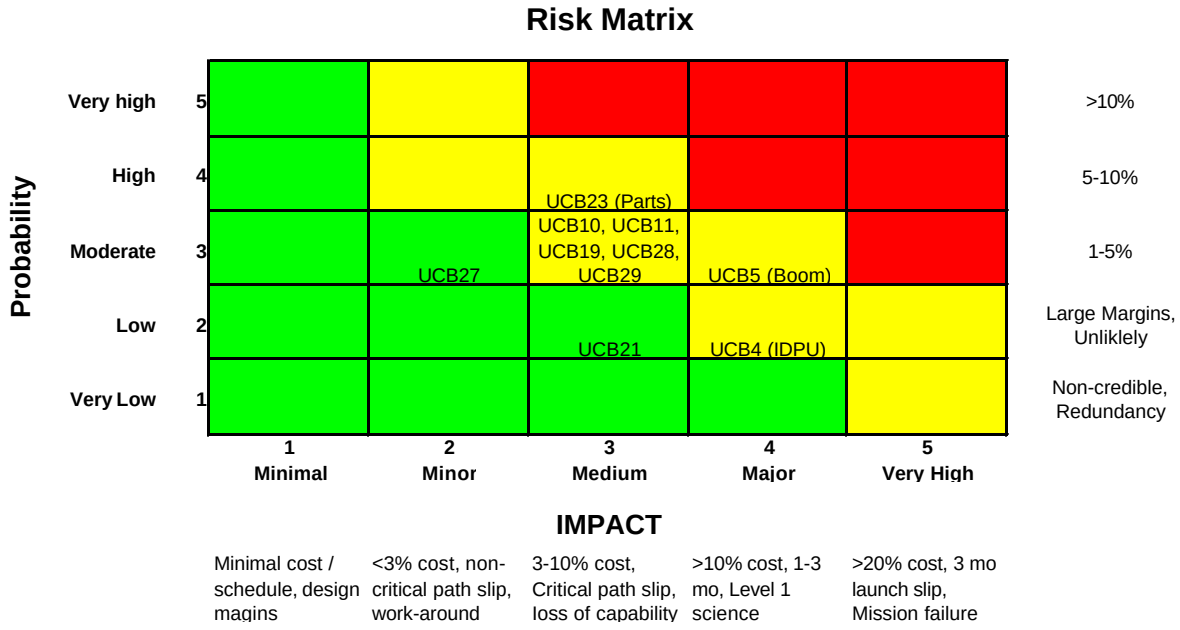
- None

1.4. *System Outstanding Issues*

- SEPT proton energy threshold not meeting requirement due to extra aluminum deposited to improve stray light rejection. Waiver submitted
- LVPS & SIT HVPS are behind schedule. Hiring people to prevent further slippage.

1.5. *Top 10 Risks*

Top 10 risks are attached. The LVPS schedule has reached the top 10 risks, and the PHASIC fell off the bottom.


Risk Matrix
Probability
Very high
5
High
4
Moderate
3
Low
2
Very Low
1
UCB23 (Parts)
UCB10, UCB11, UCB19, UCB28, UCB29
UCB27
UCB5 (Boom)
UCB21
UCB4 (IDPU)
>10%
5-10%
1-5%
Large Margins, Unliklely
Non-credible, Redundancy
1 Minimal
2 Minor
3 Medium
4 Major
5 Very High
IMPACT
Minimal cost / schedule, design magins
<3% cost, non-critical path slip, work-around
3-10% cost, Critical path slip, loss of capability
>10% cost, 1-3 mo, Level 1 science
>20% cost, 3 mo launch slip, Mission failure

IMPACT Top Ten Risks 1/2003

No.	Risk Item	Score	Mitigation	Mitigation Schedule						
				PDR	EM Test	CDR	Sub-system Test	System Test	Env test	Early Orbit Test
UCB_5	IMPACT boom is a new design. Failure could affect Imager pointing requirements as well as boom-mounted instruments.	MEDIUM	Design for reliability. Early prototype testing. Adequate force margins.	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	LOW
UCB_4	The IDPU is a single point failure mechanisim for the IMPACT suite and PLASTIC	MEDIUM	IDPU is a simple, reliable system. Extra attention will be paid to ensuring its reliability, minimizing the risk of fault propagation. Early prototype testing; extensive FM testing	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM
UCB_23	Non-standard parts qualification failure could impact delivery schedule	MEDIUM	Early parts selection and screening	MEDIUM	MEDIUM	MEDIUM	LOW	LOW	LOW	LOW
UCB_27	Actel timing differences between flight & ETU parts may cause failures late in testing impacting delivery schedule	MEDIUM	Do FM Thermal Vac early to allow time for finding and fixing timing problems; for designs on the critical path, consider installing a flight Actel in the ETU & thermal cycle.	MEDIUM	MEDIUM	MEDIUM	MEDIUM	LOW	LOW	LOW
UCB_11	Stringent EMI requirements may delay schedule if testing fails	MEDIUM	Careful design, ETU power converter testing, early system testing	MEDIUM	MEDIUM	MEDIUM	MEDIUM	LOW	LOW	LOW
UCB_28	Thermal limitations of detectors result in a low bakeout temperature which might require a very long bakeout impacting delivery schedule	MEDIUM	Bakeout subsystems prior to detector integration to reduce time of instrument-level bakeout; early bakeout	MEDIUM	MEDIUM	MEDIUM	MEDIUM	LOW	LOW	LOW
UCB_19	Concern about fragility of ITO surfaces required to meet ESC requirements; failure will impact SWEA science	MEDIUM	Replace ITO with more robust solution where possible; test ITO surfaces during I&T and replace when required	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	LOW
UCB_10	Complex Interlocking IMPACT schedule increases risk of late delivery to spacecraft	MEDIUM	Detailed fully integrated schedule developed and maintained with Project support. Monthly tracking of status.	MEDIUM	MEDIUM	MEDIUM	MEDIUM	LOW	LOW	LOW
UCB_29	LVPS behind schedule, on critical path; further slipping could delay delivery to spacecraft	MEDIUM	Add manpower to LVPS task to avoid further slippage	MEDIUM	MEDIUM	MEDIUM	LOW	LOW	LOW	LOW
UCB_18	LET Detectors from a new process	LOW	Backup L1 detectors; low risk, meet requirements; Decision point 1/2003	MEDIUM	LOW	LOW	LOW	LOW	LOW	LOW

2. Berkeley Status

2.1. *Summary of Status*

The IMPACT schedule is in the process of a rebaselining effort to reflect the changes being made to recover schedule slack.

2.2. *Major Accomplishments*

SWEA/STE:

- SWEA/STE boards fabricated, loaded, and in test.
- SWEA/STE FPGA test in progress.
- STE door life tests in progress

IDPU:

- DCB ETU#2 voltage and temperature stress tests complete
- Flight Software: Build #2: STE test complete, SWEA coding started

LVPS/HVPS:

- IDPU LVPS load/test in progress
- SIT HVPS in re-design to accommodate changed requirements
- Detailed designs for SWEA, SEP, and PLASTIC LVPS complete. Layout waiting for results from IDPU ETU tests.

Boom:

- Broken Boom stiffness measured
- Deployed boom frequency measured
- FM Tube purchase order in process
- Updating parts drawings with lessons learned from ETU in progress

GSE:

- SWEA/STE IDPU simulator GSE software complete
- MAG science module in progress
- IDPU simulator delivered to Caltech. All simulators now delivered.

2.3. *Design Updates*

- Changes to accommodate a new DAC in SWEA/STE pending results of radiation tests

2.4. *Outstanding Problems*

- ADC SEL latent damage issue. SEL test performed, results look good but analysis not complete. Further testing may be required.

2.5. *New Problems*

2.6. *Top Risks.*

ADC Latent damage issue (see above).
DAC failure impact on cost, schedule
LVPS behind schedule

2.7. *Problem/Failure Quick Look*

None.

3. GSFC (SEP) Status

Nothing to report

4. Kiel (SEPT) Status

December 2002

4.1. *Summary of Status*

1. Support given for door opening mechanism analysis. Final report due in January 2003.
2. Support given for mechanical analysis. Final report due in January or February 2003.
3. Design details for sensor housing completed: pinpuller cable routing, purge gas flow regulator location.
4. Progress made with parts testing and screening.
5. Analog and digital boards populated 80 %.

4.2. *Major Accomplishments*

a) As a result from the SEPT Door Peer Review, a mechanism analysis was requested to ensure sufficient safety margins. The analysis was contracted out and support was given.

b) To minimize the risk associated with a protoflight approach, a mechanical analysis for SEPT was contracted out. The SEPT mechanical data package to support this contract can be found at:
http://www.ieap.uni-kiel.de/space/project/stereo/sept/notes/texts/housing.pdf.
FEM analysis of SEPT in progress. First results do not show any particular concern.

c) We have proposed to place the purge flow restrictor at the tie-down for the crossover from the S/C purge hose to the instrument purge hose. This has minimum weight impact. Also, the wire routing for the pinpuller cable from the 9-pin Cannon D subminiature connector and the thermostat and heater cable from the 9-pin MDM microminiature connector has been specified.

d) Tests have been performed to characterize the PDFEs used for the EM.

e) TID Radiation testing: LMC6062AIM (+ backup part MAX478EUA), ADG713BRU (+ backup part MAX4658EUE), ADG704. Preliminary results show only some concerns about the op-amps, another part TLC2262 has been ordered as a third backup. Final reports are not yet delivered. SEE tests have not yet started.

f) High voltage and high value resistors (5.11, 10 and 190 MegaOhm) ordered by IMS, proper screening will be performed by the MASER company (Dutch)
   a. RCI-0805-5104J
   b. RCI-0805-1005J
   c. RCC-0805-1906J

g) ESA/SCC18 MHz crystal will be procured by C-MAC. The 4 MHz crystal procurement is still not closed but C-MAC HC49-4H/3L + upscreening have been approved by R. Jackson, we are investigating this possibility. We hope that our new design, requiring no 4 MHz crystal for the PDFE will work, closing then the crystal procurement issue.

h) Analog and digital boards with 80 % parts populated. Engineering model RAM not yet delivered.

i) The delivery of the electronics to Kiel is now foreseen on the 27th January 2003.

4.3. *Design Updates*

4.4. *Outstanding Problems*

4.5. *New Problems*

1. A problem with the contract for the PDFE has led to a delay in the start of the flight lot manufacturing. A new planning (with production only for SEPT) has been issued by the IMEC company, but the final T0 is still undefined and depends on the final signature of the contract. The best case would be that the contract will be in place end of January with delivery in mid-June. A re-baselined planning should be delivered soon after agreement with Kiel.

4.6. *Top Risks*

4.7. *Problem/Failure Quick Look*

5. Caltech/JPL (SEP) Status

5.1. *Summary of Status*

Activities centered on detector development, electronics development, and flight and GSE software development.

5.1.1. Major Accomplishments:

Detectors:

- The etching of the last of patterned L1 detector wafers that Micron delivered to JPL was in process at the end of the month and should be completed the first week in January. Micron is currently making additional front-side-implanted L1 wafers to send to JPL.
- The two prototype L1 detectors made from 20 micron wafers (plan B) and the two prototype H3 detectors were inspected at JPL to document problems with wire bonds and conductive epoxy contacts and were then returned to Micron for further work and testing. Micron agrees that the wire bonding needs to be improved and is developing a jig that will give the thin L1 detectors better support during the bonding.
- Micron has rejected the L1 detector mounts that have been delivered to them from GSFC due to problems with wire bonding to the contacts on these mounts. The inspection of the two prototype detectors at JPL also indicated problems with the contacts: copper was showing through the gold plating in a location close to the wire bonds.
- New mounts for H1, L2, and L3 detectors were delivered by Rigiflex, a company that produced good detector mounts for ACE. These are now in inspection at GSFC. Micron is prepared to install prototype detectors promptly upon delivery to them---detectors have been ready in chip form since April 2002.
- A meeting with Micron personnel has been scheduled for January 16-17 at Caltech to discuss status and schedule for the completion of LET and HET prototype detectors and for production of flight devices.

Electronics:

- Built a hybrid tester board for GSFC and sent it to them along with the EM hybrid and the Actel that plugs into the MISC test fixture and runs the hybrid tester board.
- Received two 8" multi-design wafers with PHASIC-2 (flight die) from AMIS.
- Lapped and diced one half of an 8" wafer netting approx. 100 PHASIC-2 die.
- The respun PHASIC die appear to be good. A single dice has been installed in a hybrid package and tested. All the "fixes" have been checked except one at this point and all seem to have worked. In particular, the glitch at linear gate opening (which was the main problem requiring a respin) has been entirely eliminated.
- Noise seems to be as expected and OK. Linearity and dynamic range likewise. The transfer function of one of the ADCs has been measured at -30, room temp and +50 C and found a gain tempco of about 40 ppm/degC, with no noticeable change in functioning over that temperature range. The tempco of the offset of the transfer function was a particularly low value of 0.01 channels per degree C. (We claimed less

than 0.1 channels per degree C in our preliminary spec.) It appears that we have robust performance over a wide temperature range.
- It is likely OK to conclude that the respin has been successful and another respin will not be needed.
- We are working to get the "thermal inducer" operating. It is on loan from JPL and will be used to quickly and easily bring a PHASIC under test to the desired test temperature (using a stream of temperature controlled dry air). The inducer requires a source of compressed air at 100 psi and fairly high volume. The plumbing to bring this into the STEREO lab is in the works. A test using compressed air available in the machine shop was successful. We will probably relocate the inducer and hybrid test setup temporarily to a location outside our lab that has the needed compressed air source to avoid impacting our hybrid test development schedule.
- A second PHASIC hybrid is ready for test and six additional EM units are being fabricated at JPL. After the testing of these parts we will adopt parameter limits, then finalize and document the hybrid tests prior to the PHASIC hybrid CDR/MRR, which is desired to occur near Jan. 20.
- The layout of the SEP Central MISC board has been started using an assumed board outline. (We are still waiting on GSFC for the "final" board outlines.)
- Built a hybrid tester board for GSFC and sent it to them along with the EM hybrid and the Actel that plugs into the MISC test fixture and runs the hybrid tester board.
- Received finalized schematics of Analog/Post-Regulator and Bias Supply boards from Space Instruments for review.
- Resources update will follow in a separate message.

Software:
- Began hardware and software development for SEP instrument simulator.

GSE:
- Completed the code for the generic page displays and time histories
- Prepared demo of the page displays and time histories for the LET rate data based on the current (Version 6.0) LET Science Format. (Work on LET event data and housekeeping has not begun.)
- Prepared demo of page displays for dumping SEP packets.
- Received both the IDPU simulator and front-end software from UCB. Have loaded the UCB software on a Windows-XP machine and briefly tested whether directives (commands) can be sent from the PC host to the IDPU simulator; telemetry flow thru the IDPU simulator to the host PC and the networking software have not yet been tested.

5.2. *Design Updates*

- Resource updates will be sent separately.

5.3. *Outstanding Problems*

- L1 thinning continues to be a challenge. We will decide on whether to switch to the backup Plan B method by 1/31/03.

5.4. *New Problems*

- None.

5.5. *Top Risks.*

- The budget is very tight with no reserve being held at Caltech.
- Schedule slack that we show explicitly will be taken away from us.
- Development of the L1 detector. Risk mitigated by creating slack in schedule and by starting a parallel development effort using different and more conventional manufacturing technique (Plan B detectors).

5.6. *Problem/Failure Quick Look*

- None.

6. SIT MONTHLY TECHNICAL PROGRESS REPORT

6.1. *SUMMARY of STATUS*

a) SIT TELESCOPE - Prototype is in house and working. Flight solid-state detectors are in house, awaiting test.
b) SIT TOF System - Flight unit 1 at GSFC. May need to be downgraded to flight spare.
c) SIT Energy/Logic System - Prototype energy system has been integrated with the prototype TOF system and is functioning at UMd. Front-end logic is being implemented at GSFC. ETU energy board is in work.
d) SIT HVPS - HVPS ETU at UMd undergoing life test. Re-design of output section underway at UCB.

6.1.1. Schedule Changes

The current SIT schedule is available from Robert Palfy

6.2. *MAJOR ACCOMPLISHMENTS*

6.2.1. This Month

- Energy Board: The ETU energy board assembly was begun.
- TOF: TOF Flight Unit 1 TOF boards were inspected at GSFC and problems were discovered.
- Logic: The prototype PWB was received and has had the socket successfully attached. It awaits final assembly to allow testing of the front-end logic Actel chip.
- HVPS: Redesign continued at UCB. ETU life test continued at UMd. This test is proceeding with no problems noted in the behavior of the HVPS.

6.2.2. Next Month

In January we intend to finish assembly and test of the ETU energy board and to begin testing the front-end logic Actel. We need to begin testing on the solid-state detectors. We expect to receive the flight micro-channel plates in January.

6.3. *DESIGN UPDATES*

6.3.1. Resources

	Last Month	This Month	Change
Mass (kg) *	1.46	1.46	0
Power (mW)**	1.36	1.36	0
Telemetry (bps)	418	418	0

* Includes 200g bookkept by GSFC for SIT structure

** Note: Mass and power increases due to measured values for ETU HVPS

6.4. *OUTSTANDING PROBLEMS*

6.5. *NEW PROBLEMS*

Inspection of the "Flight Unit 1" TOF boards at GSFC has uncovered a number of problems of varying severity. We need to evaluate these problems and identify changes needed to bring these and/or the following TOF boards to flyable status.

6.6. *NEW RISKS*

6.7. *PROBLEM/FAILURE QUICK LOOK*

Starts at first turn-on of flight hardware.

ID #	Description	Assignee	Opened	Closed

7. CESR (SWEA) Status

CESR- TOULOUSE- France **Author : Claude Aoustin / Project Manager**

SWEA PROGRESS REPORT # 15
(January 17, 2003)

December 2002

CESR is in charge of :

- Electrostatic analyzer with deflectors, grids and Retractable Cover
- Detector consisting of two MCP rings
- Amplifiers and discriminators
- 3 High voltages

7.1. *Summary of Status*

CDR took place 20-22 November

7.1.1. ETU1

Delivery to UCB was planned for 12/07/2002 : done 26/09/2002

7.1.2. ETU2

Mechanical fabrication 100 % done
Integration on going.
Electronic boards received : under test

7.2. *Major accomplishments*

ETU2 fabrication
Mechanical fabrication :
All the mechanical pieces are fabricated
Spheres surface treatment done.
Surface treatment (gold, nuflon) done.
Grids delivered.
Cover opening mechanism ready and tested.
Mechanical integration started.
Electronics :
HV coupling board received.
HV board received and under test.
Amplifiers board received under population.

7.3. *Design Updates*

Mass : 1040 g (EM is 950g without cover opening mechanism)
Power : 446 mW min ; 662 mW max

7.4. *Outstanding Problems*

AMPTEKS amplifiers quality:
- additional burn in will be done : 1000h at 125°C on 10 pieces.
- burn in test performed.

7.5. *New problems*

None

7.6. *Top Risks*

7.7. *Problem Failure Quick Look*

None

8. GSFC (MAG) Status

Nothing to report.

9. EPO at UCB

Monthly E/PO Report

December, 2002

AGU Fall Meeting:

A poster, *High "IMPACT" STEREO E/PO: Exploiting Opportunities for High Visibility Activities On a Shoestring*, was presented for the Fall meeting of the American Geophysical Union in San Francisco, CA.

Formal Education:

Background work was done for a web-based curriculum piece on the STEREO/IMPACT boom. An idea was formed to create tutorials for both the students and teachers giving background information on magnetism.

Respectfully Submitted,

STEREO/IMPACT E/PO scientists Nahide Craig and Bryan Méndez