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Subject: IMPACT Monthly Technical Progress Report, Contract NAS5-00133

Harry:

Enclosed is the monthly technical progress report for the STEREO IMPACT project for the month of November 2002.

Sincerely,

David Curtis
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CC:

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IMPACT Team

1. IMPACT Overview

This report is presented in sections by institution. Section 1 is an IMPACT Project Manager / System Engineer's overview.

1.1. *Contracting / Funding*

Funding to the end of CY02 is in place. Because of pipe-line delays in the system through to the subcontractors (Caltech and UMd) it is important that IMPACT be funded somewhat in advance of expected spending.

There have been a significant number of items agreed upon between IMPACT and Project that involve incremental funding. We need to mod the contract to reflect those changes. The first step is to agree upon what those changes are, which is in progress.

1.2. *Significant System-Level Accomplishments*

- Held peer review on SIT door mechanism.
- Developed and presented the IMPACT Instrument CDR
- Participated in the PLASTIC CDR (LVPS, IDPU Software)
- Delivered Boom test plan for review
- Updated IMPACT Harness spec
- Updated SWEA ICD

1.3. *System Design Updates*

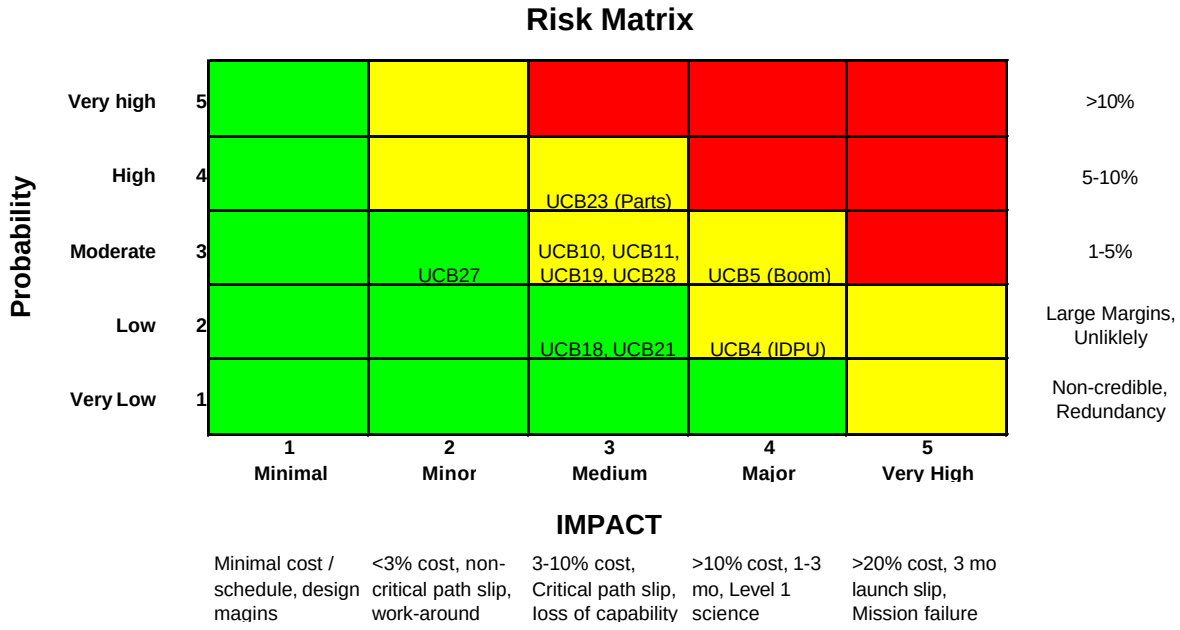
- None

1.4. *System Outstanding Issues*

- SEPT proton energy threshold not meeting requirement due to extra aluminum deposited to improve stray light rejection. Waiver submitted
- STE radiation source waiver Approved
- Operational heater power budget over allocation. Waiver to allocations submitted.
- Added power for change to less SEU-sensitive RAMs in IDPU. Waiver subitted.

1.5. *Top 10 Risks*

Top 10 risks are attached. A new method of evaluating risks has been applied (5x5 instead of 3x3). As a result the risk codings are lower (no Red risks).


Risk Matrix
Probability
Very high
5
High
4
Moderate
3
Low
2
Very Low
1
UCB23 (Parts)
UCB27
UCB10, UCB11, UCB19, UCB28
UCB5 (Boom)
UCB18, UCB21
UCB4 (IDPU)
>10%
5-10%
1-5%
Large Margins, Unliklely
Non-credible, Redundancy
1 Minimal
2 Minor
3 Medium
4 Major
5 Very High
IMPACT
Minimal cost / schedule, design magins
<3% cost, non-critical path slip, work-around
3-10% cost, Critical path slip, loss of capability
>10% cost, 1-3 mo, Level 1 science
>20% cost, 3 mo launch slip, Mission failure

IMPACT Top Ten Risks 11/2002

No.	Risk Item	Score	Mitigation	Mitigation Schedule						
				PDR	EM Test	CDR	Sub-system Test	System Test	Env test	Early Orbit Test
UCB_5	IMPACT boom is a new design. Failure could affect Imager pointing requirements as well as boom-mounted instruments.	MEDIUM	Design for reliability. Early prototype testing. Adequate force margins.	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	LOW
UCB_4	The IDPU is a single point failure mechanisim for the IMPACT suite and PLASTIC	MEDIUM	IDPU is a simple, reliable system. Extra attention will be paid to ensuring its reliability, minimizing the risk of fault propagation. Early prototype testing	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM
UCB_23	Non-standard parts qualification failure could impact delivery schedule	MEDIUM	Early parts selection and screening	MEDIUM	MEDIUM	MEDIUM	LOW	LOW	LOW	LOW
UCB_27	Actel timing differences between flight & ETU parts may cause failures late in testing impacting delivery schedule	MEDIUM	Do FM Thermal Vac early to allow time for finding and fixing timing problems; for designs on the critical path, consider installing a flight Actel in the ETU & thermal cycle.	MEDIUM	MEDIUM	MEDIUM	MEDIUM	LOW	LOW	LOW
UCB_11	Stringent EMI requirements may delay schedule if testing fails	MEDIUM	Careful design, ETU power converter testing, early system testing	MEDIUM	MEDIUM	MEDIUM	MEDIUM	LOW	LOW	LOW
UCB_28	Thermal limitations of detectors result in a low bakeout temperature which might require a very long bakeout impacting delivery schedule	MEDIUM	Bakeout subsystems prior to detector integration to reduce time of instrument-level bakeout; early bakeout	MEDIUM	MEDIUM	MEDIUM	MEDIUM	LOW	LOW	LOW
UCB_19	Concern about fragility of ITO surfaces required to meet ESC requirements; failure will impact SWEA science	MEDIUM	Replace ITO with more robust solution where possible; test ITO surfaces during I&T and replace when required	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	LOW
UCB_10	Complex Interlocking IMPACT schedule increases risk of late delivery to spacecraft	MEDIUM	Detailed fully integrated schedule developed and maintained with Project support. Monthly tracking of status.	MEDIUM	MEDIUM	MEDIUM	MEDIUM	LOW	LOW	LOW
UCB_21	PHASIC Custom VLSI used in SEP may has schedule and cost risk	LOW	Early development to prove design; use Amptek in place of VLSI in SIT (stll use VLSI in HET, LET); first run looks good, but a second run will be required	MEDIUM	LOW	LOW	LOW	LOW	LOW	LOW
UCB_18	LET Detectors from a new process	LOW	Backup L1 detectors; low risk, meet requirements; Decision point 1/2003	MEDIUM	LOW	LOW	LOW	LOW	LOW	LOW

2. Berkeley Status

2.1. *Summary of Status*

The IMPACT schedule is in the process of a rebaselining effort to reflect the changes being made to recover schedule slack.

2.2. *Major Accomplishments*

SWEA/STE:

- SWEA/STE boards fabricated, loaded, and in test.
- SWEA/STE FPGA test in progress.
- STE box/door ETU fab complete & door mechanism tested (it works!)

IDPU:

- DCB ETU#2 configured for voltage and temperature stress tests.
- Flight Software: Build #2: Tests in progress.

LVPS/HVPS:

- IDPU LVPS load/test in progress
- SIT HVPS in re-design to accommodate changed requirements
- Detailed designs for SWEA, SEP, and PLASTIC LVPS complete. Layout waiting for results from IDPU ETU tests.

Boom:

- Thermal joint test completed. Joints seem to survive fine. Epoxy for joint selected.
- ETU boom tubes & joints complete and tested. Deployment tests performed
    - Some machining errors prevent the joints from completely locking up (5 out of 6 pins lock per joint).
- Force margins measured.
    - It looks like existing stacer is inadequate; a new stronger one will be required.
- Custom harness material has been delivered and is in test (stacer requirements pending this result).
- Testing results of ETU have led to changes in the design that cannot be incorporated in the ETU. We are no longer planning a full set of environmental tests on the ETU. The next model (Qual/Fight Spare) shall get the full set of environments.

GSE:

- SWEA/STE IDPU simulator GSE software complete
- MAG science module in progress
- IDPU simulator hardware being prepared for Caltech (SEP)

2.3. *Design Updates*

- Changes to the details of the boom design as a result of ETU testing as indicated above.

2.4. *Outstanding Problems*

- ADC SEL latent damage issue. SEL test performed, results look good but analysis not complete. Further testing may be required.

2.5. *New Problems*

- DAC radiation failure. This part is used by the SWEA/STE interface. It failed disastrously at 8krads. A new part will have to be selected. This will involve a new ETU of the SWEA/STE interface, a change to the Actel design, and probably screening of a new part.

2.6. *Top Risks.*

ADC Latent damage issue (see above).
DAC failure impact on cost, schedule

2.7. *Problem/Failure Quick Look*

None.

3. GSFC (SEP) Status

STEREO/IMPACT/SEP/GSFC Progress Report for November, 2002 – (von Rosenvinge, Baker, Hawk, Reames, Shuman, Wortman)

3.1. *Summary of Status -*

We have submitted new orders for L2, L3, and H1 detector mounts to Rigiflex. As explained in the September report, Rigiflex was originally substantially underbid for these mounts. We have been forced to go with Rigiflex because the first contractor failed to build these mounts to our specifications. Twenty H1 detector mounts have already been received from Rigiflex. They have passed coupon inspections. Fifteen passed QA inspection; 5 have not yet been accepted due to some bare spots in the Au coating where the connectors are to be soldered. If the bare spots are exposed copper and connectors solder successfully then these 5 mounts will also be accepted. Dimensional inspection and attachment of connectors remain before these can be sent to Micron. The L2 and L3 mounts are expected presently.

3.2. *Major Accomplishments*

- Participated in a Peer Review for the SIT door mechanism (Nov 15).
- Completed an initial vibration analysis of SEP Main (includes SEP Central, LET, and HET). The primary finding is that the mounting feet may need to be separated by an additional inch in order to reduce the pull-force on the inserts in the spacecraft honeycomb panel. It was found at about the same time that the Low Voltage Power Supply needs additional space. These two taken together are necessitating a revision to the SEP Main ICD drawing which was submitted this month.
- Completed and presented 5 different presentations for the IMPACT Critical Design Review (Nov 20 – 22).
- Completed a C-version of the HET on-board particle identification algorithm and translated it to 24-bit assembly code. Also completed assembly code for the event queuing algorithm.
- Completed a GSE Software User's Guide, Build 1.
- Delivered a MISCless version of the SIT front-end electronics ASIC to Peter Walpole at U of MD.
- Submitted a waiver request to use Shin-Etsu Adhesive KJR-9022E on Micron Detectors.

3.2.1. Next Month-

- Complete SEPT and SEP Main ICD drawing changes
- Work on HET Particle Identification tables
- Complete revised schedule

3.3. *Design Updates*

Mass impact of changes to SEP Main resulting from the design changes discussed above are being determined now.

3.4. *Outstanding Problems*

Problems with obtaining detector mounts were discussed above.

3.5. *New Problems*

None.

3.6. *Top Risks*

No significant risks at GSFC? Need to ensure that manpower becomes available per the current plan.

3.7. *Problem/Failure Quick Look*

4. Kiel (SEPT) Status

November 2002

4.1. *Summary of Status*

1. Support for and participation in IMPACT CDR.
2. Delivery of all five magnet systems from Vacuumschmelze (1 EM and 4 FM).
3. Foil carrier rings fabricated, Alodine 1200 surface treatment applied, fabrication of Parylene foils ordered.
4. Delivery of pinpullers from TiNi overdue (should be delivered in October).
5. Data Package for mechanical analysis finished. Analysis contracted out.
6. Mechanism analysis contracted out.
7. EM boards design took more time than expected (grounding problem). Current delay: 2 weeks, hope to decrease the delay to 1 week.

4.2. *Major Accomplishments*

1. We have now 6 magnet systems inhouse: 1 prototype, 1 EM and 4 FM. Incoming inspection ongoing. Far field of EM/FM systems better by factor 3 compared to prototype. Prototype was already found acceptable by Mario Acuna.
2. Contracts for mechanical analysis for SEPT and separate analysis for mechanism are placed with companies in the Netherlands and Germany, respectively.
3. EM electronics layout finished.
4. PDFE redesign finished (contract approved)
5. The PDFE test bench (to tune individually each PDFE) design has been initiated. The board will use the first version of the FPGA which can control a DAC and each PDFE. The DAC (12 bits, 8 outputs) will be used to produce the voltage and current biases needed for each PDFE. The aim of this board is to find the optimum of the tuning of each PDFE.
6. 50 Ohm resistor in the interface circuitry has been moved to another location. This change will be implemented on the EM.
7. Power supply GSE development: design specification document written for KTH institute.
8. Debugging on BB2 (breadboard 2) at KTH is progressing.
9. PDFE testing in ESTEC is progressing (tuning+ acquisition of new spectrum with BB1). A correction of the differential linearity for the PDFE has led to improvement of the spectra w.r.t. the first acquisitions.
10. FEM analysis of SEPT (+ bracket) has been started. First results expected in mid January 2003.
11. SEPT Operation Control and Data Processing Requirements Doc. updated, release early December 2002.
12. Debugging on BB2 (breadboard 2) at KTH is progressing.
13. BB1 characterization still ongoing.
14. Radiation testing started on two parts. All the tests will be finished by mid December 2002. Reports will be written.
15. Analog board and EMI shield EM board delivered. Digital board expected 1st week of December.

16. High voltage and high value resistors (5.11, 10 and 190 MegaOhm). CRHV Vishay resistors not available with 1206 or inferior size. Alternative manufacturer has been found with IMS:
    a. RCI-0805-5104J
    b. RCI-0805-1005J
    c. RCC-0805-1906J
    d. The screening will be performed by IGG Component Technology
    e. We are waiting for the quotation
17. Crystal manufacturer has been identified. Parts have been ordered for study and screening.

4.3. *Design Updates*

4.4. *Outstanding Problems*

1. Thermal hardware needs to be specified: type of operational heater, survival heater.
2. Who is responsible for providing and implementing the various components of thermal hardware including thermally isolating Ultem bushing, MLI, and thermal paint?

4.5. *New Problems*

4.6. *Top Risks*

4.7. *Problem/Failure Quick Look*

5. Caltech/JPL (SEP) Status

5.1. *Summary of Status*

Activities centered on preparation of CDR materials, CDR presentations, detector development, electronics development, and flight and GSE software development.

Major Accomplishments:

Programmatic:

- We participated in the IMPACT CDR held in Greenbelt, MD 20-22 November 2002. The preparation of the materials presented at CDR and the materials required for delivery at the time of CDR occupied many of us for much of October and the first two weeks of November.

Detectors:

- Thus far, a total of four silicon wafers that have been etched down for the production of L1 detectors have been delivered to Micron Semiconductor for inspection and evaluation. The first two of these were rejected due to damage to implants on the front (non-etched) side of the wafer when the etchant broke through on some test areas. The two additional wafers etched after the test areas had been masked off to avoid this problem were also rejected by Micron. Oxides, which Micron had grown on the wafer, were inadvertently removed during cleaning following the apparently successful etching. Micron also reported some tiny (100 micron or less diameter) pinholes in the thinned areas. These two wafers are being sent back to JPL for inspection in order to understand this problem. One more wafer is currently in the process of being etched.
- Micron delivered two prototype L1 detectors made from 20 micron lapped and polished wafers ("plan B" detectors) in flight-approved mounts. The thickness uniformity was measured at Caltech and found to meet the LET requirement (<0.6 micron rms variation) for both detectors. These two detectors did not function electrically when they were delivered. Inspection revealed problems with the contacts. A sizeable number of wire bonds had separated or broken. In addition, there was a problem with the back side contacts (one per detector) Micron had made using a fairly thick wire connected using conductive epoxy. Preliminary inspection indicated that the epoxy had lifted from the detector surface and/or cracked, possibly due to the wire being too stiff. This back side contact was made using conductive epoxy rather than by wire bonding as planned because Micron was finding wire bonding on the back side of the detectors, where there is no support ledge, was causing breakage of the thin silicon. Micron is designing a support fixture that should allow wire bonding on future L1 devices.
- Micron also delivered two prototype H3 detectors in flight-approved mounts. One of these could also not be tested electrically because all of the wire bonds on the front side (3 total) had lifted from the circuit-board mount. The L1 and H3 detectors are being inspected by a wire-bonding expert at JPL to document and understand the nature of the bond failures and improve the process on future detectors. The non-

functioning devices will then be shipped back to Micron for their evaluation and repair.
- Some initial tests were made of the one H3 detector that did have electrical continuity. The leakage current as a function of bias and the alpha particle resolution satisfy HET requirements.

Electronics:
- We have a working PHASIC hybrid that uses a non-flight original VLSI chip. We are working toward getting a respun chip into a hybrid.
- We developed a way to operate the MISCs at lower power. A software command now can gate off the clock, which automatically ungates on the next interrupt. This technique is clearly good for the SEP central MISC, which has a continuous low CPU utilization rate and should see a steady power reduction near 70%. For the other MISCs (LET, HET, and SIT) the average power will drop by a similar amount, but peak power will drop a lesser amount depending on the peak CPU utilization rate in flares. However, since we anticipate a CPU utilization rate of only about 50% even in flares (for LET), the peak power should still drop about 35%.
- Offsetting the power reduction is the possibility of higher power consumption for the flight Actels relative to the commercial ones on which our power estimates are currently based. We are currently working to redo the power estimates taking into account both effects.
- Much progress on ICDs was made with near-final versions out for review.
- Schematic capture is nearly complete for the LET front-end/MISC board and SEP Central logic board. Layout is about to begin.
- We received a thermal inducer from JPL and have been working to get a source of clean compressed air needed to operate it. The unit will be used for temperature testing of the PHASIC hybrids.
- Space Instruments fabricated and tested the new version of the Bias Supply. The combination of the Bias Supply and the High Voltage Post Regulators was tested. Power estimates were updated based on the measurements on the proof of concept boards.
- Space Instruments provided new updates related to the Bias Supply and the Analog/Post-reg board for the schematics and parts lists. Connector information was added to the schematics for the Analog/Post-reg Board.

Software:
- Wrote final version of LET/SEP_Central Software Requirements Doc.
- Worked on onboard data processing algorithms for LET.

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GSE:
- Finished writing (not tested) most (90%) of code for displaying generic page displays and time time histories. Code will be completed and tested with simplistic pseudo data next month. (Note: Code to extract actual LET and SEP structures for the final page displays and time histories is not due until March 2003.)
- Java code for handling elapsed seconds 1958 (time system used in the CCSDS packets) has been completed and partially tested.
- First GSE computer has been specified and ordered.

5.2. *Design Updates*

- Resource updates will be sent separately.

5.3. *Outstanding Problems*

- L1 thinning continues to be a challenge. We will decide on whether to switch to the backup Plan B method by 1/31/03. It would be helpful schedule-wise to invest some dollars to get some Plan B wafers ordered soon. We are contacting Micron to see what funding is required.

5.4. *New Problems*

- None.

5.5. *Top Risks.*

- The budget is very tight with no reserve being held at Caltech.
- Schedule slack that we show explicitly will be taken away from us.
- Development of the L1 detector. Risk mitigated by creating slack in schedule and by starting a parallel development effort using different and more conventional manufacturing technique (Plan B detectors).

5.6. *Problem/Failure Quick Look*

- None.

6. SIT MONTHLY TECHNICAL PROGRESS REPORT

6.1. *SUMMARY of STATUS*

a. SIT TELESCOPE - Prototype is in house and working.

b. SIT TOF System - Flight unit 1 in house, tested in Germany, awaiting testing at UMd

c. SIT Energy/Logic System - Prototype energy system has been integrated with the prototype TOF system and both are under test with GSE logic board. Front end logic is being implemented at GSFC. ETU energy board is in work.

d. SIT HVPS - HVPS ETU at UMd undergoing life test. Redesign of output section underway at UCB.

6.1.1. Schedule Changes

The current SIT schedule is available from Robert Palfy

6.2. *MAJOR ACCOMPLISHMENTS*

6.2.1. This Month

Logic : A new layout for the logic test board was prepared to make it easier to assemble the socket to the board. A vendor has been found to do the assembly. The updated PCB is expected in mid December. Prototyping Actel parts were ordered and received. The front-end logic was implemented in Actel from UMD specifications by George Winkert at GSFC and the Actel is at UMd waiting test.

HVPS: The ETU HVPS was received at UMd and tested with the prototype telescope and electronics. It was discovered that the output voltages were not as required, due in part to inadequate specifications. A new specification was written and delivered to UCB and design work is underway to make the necessary changes.

Software: Kristin Wortman and Tom Nolan have made significant progress in implementing the event handling software and in defining the interrupt routines. This work continues at GSFC.

Reviews: Supported CDR

6.2.2. Next Month

In December we hope to assemble and begin testing on the test logic board. We also will begin assembly of the ETU energy board with flat-pack Amptek hybrids, preparatory to releasing flight layout for fabrication in January.

6.3. *DESIGN UPDATES*

6.3.1. Resources

	Last Month	This Month	Change
Mass (kg) *	1.34	1.46	0.12
Power (mW)**	1.35	1.36	0.01
Telemetry (bps)	418	418	0

* Includes 200g bookkept by GSFC for SIT structure

** Note: Mass and power increases due to measured values for ETU HVPS

6.4. *OUTSTANDING PROBLEMS*

6.5. *NEW PROBLEMS*

6.6. *NEW RISKS*

6.7. *PROBLEM/FAILURE QUICK LOOK*

Starts at first turn-on of flight hardware.

ID #	Description	Assignee	Opened	Closed

7. CESR (SWEA) Status

CESR- TOULOUSE- France **Author : Claude Aoustin / Project Manager**

SWEA PROGRESS REPORT # 14
(December 16, 2002)

November 2002

CESR is in charge of :
- Electrostatic analyzer with deflectors, grids and Retractable Cover
- Detector consisting of two MCP rings
- Amplifiers and discriminators
- 3 High voltages

7.1. *Summary of Status*

7.1.1. ETU1

Delivery to UCB was planned for 12/07/2002 : done 26/09/2002

7.1.2. ETU2

Mechanical fabrication 90 % done
Electronic boards under fabrication

CDR took place 20-22 November

7.2. *Major accomplishments*

ETU2 fabrication
Mechanical fabrication :
All the mechanical pieces are fabricated
Spheres surface treatment done.
Surface treatment (gold, nuflon) on the way.
Grids under fabrication.
Cover opening mechanism ready and tested.
Electronics :
Printed circuits boards under fabrication

7.3. *Design Updates*

Mass : 1040 g (EM is 950g without cover opening mechanism)
Power : 446 mW min ; 662 mW max

7.4. *Outstanding Problems*

AMPTEKS amplifiers quality:
- additional burn in will be done : 1000h at 125°C on 10 pieces.
- under test at Hirex : subcontractor specialized for testing flight parts.

7.5. *New problems*

None

7.6. *Top Risks*

7.7. *Problem Failure Quick Look*

None

8. GSFC (MAG) Status

Nothing to report.

9. EPO at UCB

Monthly E/PO Report

November, 2002

Public Outreach:

- The STEREO/IMPACT website was edited and updated with new news and events and a reworked K-12 Curriculum page.
- Work has continued on the *Sounds of Space* website. The original website, *Voice of Space*, was modified to incorporate it within the STEREO/IMPACT E/PO site.

AGU Fall Meeting:

A poster for the AGU 2002 fall meeting, *High "IMPACT" STEREO E/PO: Exploiting Opportunities for High Visibility Activities On a Shoestring*, was prepared for presentation on 6 December 2002.

Formal Education:

Background work was done for a web-based curriculum piece on the STEREO/IMPACT boom. We investigated state and national science standards that could be met by the activity.

Respectfully Submitted,

STEREO/IMPACT E/PO scientists Nahide Craig and Bryan Méndez