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Subject: IMPACT Monthly Technical Progress Report, Contract NAS5-00133

Harry:

Enclosed is the monthly technical progress report for the STEREO IMPACT project for the month of September 2002.

Sincerely,

David Curtis
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CC:

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IMPACT Team

1. IMPACT Overview

This report is presented in sections by institution. Section 1 is an IMPACT Project Manager / System Engineer's overview.

1.1. *Contracting / Funding*

Funding to the end of FY02 is in place. Because of pipe-line delays in the system through to the subcontractors (Caltech and UMd) it is important that IMPACT be funded somewhat in advance of expected spending. We will need funding in October to avoid running out of funds.

1.2. *Significant System-Level Accomplishments*

- Held peer reviews on SWEA and SEPT door mechanisms.
- Visited ESTEC to discuss the status of SEPT work there
- Participated in a 3-day NASA Survey at UCB
- Participated in a boom progress review at UCB
- Reorganized boom effort and added manpower to meet desired level of ETU fabrication and test by CDR
- Provided input to Project Mechanisms list

1.3. *System Design Updates*

- None

1.4. *System Outstanding Issues*

- SEPT proton energy threshold not meeting requirement due to extra aluminum deposited to improve stray light rejection. Waiver submitted
- STE radiation source has not been approved yet by Project. Waiver submitted
- Operational heater power budget over allocation. Waiver to allocations submitted.
- Added power for change to less SEU-sensitive RAMs in IDPU. Waiver subitted.

1.5. *Top 10 Risks*

Top 10 risks are attached. A new risk (UCB_026) is related to the Analog to Digital Converter being used by IMPACT, PLASTIC, and SWAVES, and being qualified by UCB. GSFC Radiation Parts Group is concerned about the possibility of latent damage caused when the part latches up (prior to the latchup protection circuit activating). They recommended some additional testing which it appears that Project will fund. If the parts are found to be unacceptable, a replacement will have to be found and qualified, and a number of designs at the ETU stage will need to be re-worked. This could have $, schedule, mass, and power implications. Some other risks have been reordered based on progress made in their mitigation.

IMPACT Top Ten Risks 9/2002

No.	Risk Item	Score	Mitigation	Mitigation Schedule						
				PDR	Bread-board Test	CDR	Sub-system Test	System Test	Env test	Early Orbit Test
UCB_5	IMPACT boom is a new design. Failure could affect Imager pointing requirements as well as boom-mounted instruments.	HIGH	Design for reliability. Early development and test to ensure reliability.	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH
UCB_26	Analog to Digital Convert SEL latent damage issue	MEDIUM	Testing planned, backup parts under investigation	MEDIUM	MEDIUM	MEDIUM	LOW	LOW	LOW	LOW
UCB_23	Non-standard parts qualification failure could impact delivery schedule	MEDIUM	Early parts selection and screening	MEDIUM	MEDIUM	LOW	LOW	LOW	LOW	LOW
UCB_15	GSFC Approval Requirements could delay instrument delivery or add cost	MEDIUM	Difficult to asses, history is mixed	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	LOW
UCB_4	The IDPU is a single point failure mechanisim for the IMPACT suite and PLASTIC	HIGH	IDPU is a simple, reliable system. Extra attention will be paid to ensuring its reliability	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH
UCB_13	IMPACT team is thin; loss of a critical team member could delay delivery	MEDIUM	Reassign work amongst team as and when required	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	LOW	LOW
UCB_11	Stringent EMI requirements may delay schedule if testing fails	MEDIUM	Careful design, early testing	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	LOW	LOW
UCB_21	Custom VLSI used in SEP may has schedule and cost risk	MEDIUM	Early development to prove design; use Amptek in place of VLSI in SIT (stll use VLSI in HET, LET); first run looks good, but a second run will be required	MEDIUM	MEDIUM	LOW	LOW	LOW	LOW	LOW
UCB_1	ITAR restriction of information exchange with foreign CoIs may result in problems not discovered until late in the program	MEDIUM	Various channels of communication have been found within the ITAR restrictions to allow adequate information flow. Some exchanges are still forbidden and may cause a problem.	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	LOW
UCB_18	LET Detectors from a new manufacturer	MEDIUM	Backup L1 dtectors ordered; low risk, meet requirements	MEDIUM	MEDIUM	LOW	LOW	LOW	LOW	LOW

2. Berkeley Status

2.1. *Summary of Status*

The UCB schedule with updated status will be delivered separately.

2.2. *Major Accomplishments*

SWEA/STE:<< (ADC)

- SWEA/STE boards fabricated, loaded, and in test.
- SWEA/STE FPGA test in progress.
- STE box/door ETU fab in progress. (Priority of this work lowered to press forward on boom efforts)

IDPU:

- Data Controller Board ETU#1 configured for software development and interface testing.
- DCB ETU#2 completed and tested. KDS version processor and UT9Q512 SRAMs on this board found acceptable
- Decision made to go with KDS processor and UT9Q512 SRAMs. A significant power increase due to the memories (2W worst case)
- Flight Software: Build #2: Tests in progress. Significant effort expended in ferreting out bugs in Spacecraft Emulator.

LVPS/HVPS:

- IDPU LVPS layout in progress
- SIT HVPS in test. Delivery in early October.
- Detailed designs for SWEA, SEP, and PLASTIC LVPS in progress.

Boom:

- Boom tubes being prepared (cut/drilled)
- Rings in fabrication, due mid October
- Joint thermal test in progress
- Peer review re-scheduled for October 29, at which time we will have completed deployment stiffness, and joint thermal tests
- Harness wire order delayed, will not deliver till mid ~~December~~ November.

GSE:

- IDPU Simulator hardware & sample software delivered to UNH (PLASTIC).
- SWEA/STE IDPU simulator GSE software in progress

2.3. *Design Updates*

- Change to KDS processor and UT9Q512K SRAMs as indicated above.
- Boom joint “fingers” added to keep joints warm in nominal spacecraft orientation

2.4. *Outstanding Problems*

- Boom thermal issue; to be resolved by joint cold test

2.5. *New Problems*

- ADC SEL latent damage issue

2.6. *Top Risks.*

ADC Latent damage issue (see above).

2.7. *Problem/Failure Quick Look*

None.

3. GSFC (SEP) Status

STEREO/IMPACT/SEP/GSFC Progress Report for September, 2002 – (von Rosenvinge, Baker, Hawk, Reames, Shuman, Wortman)

3.1. *Summary of Status*

We are encountering problems. Four HET H3 and ten LET L1 detector mounts have been sent to Colin Wilburn at Micron and more are available. However several attempts to obtain completed LET L2, LET L3 and HET H1 detector mounts have failed, either in mechanical inspection or in coupon inspection. We are therefore submitting a request for a requote to Rigiflex. Earlier quotes from Rigiflex were about double the quotes from other companies, however we have had prior excellent experience with them on ACE, and we are running out of time.

3.2. *Major Accomplishments*

- A problem which was earlier identified with our prototype Caltech ASIC test setup has been resolved. The ASIC chip is performing very well.
- The SIT on-board particle identification algorithm has been coded from a Fortran version to a MISC assembly language version and it performs correctly on the MISC.
- The first iteration of the SIT front-end electronics design has been completed.

3.2.1. Next month

- Continue work on the overall SEP mechanical design, including the SIT door.
- Continue work on the HET GSE.
- Complete a C-version of the HET on-board particle identification algorithm.
- Deliver a MISCless version of the SIT front-end electronics ASIC to Peter Walpole at U of MD.
- Prepare for the CDR in November.

3.3. *Design Updates*

None quantified this month.

3.4. *Outstanding Problems*

Problems with obtaining detector mounts were discussed above.

3.5. *New Problems*

None.

3.6. *Top Risks*

No significant risks at GSFC? Need to ensure that manpower becomes available per the current plan.

3.7. *Problem/Failure Quick Look*

4. Kiel (SEPT) Status

No report provided for September.
Summary of Kiel information obtained at Door Peer Review:

- Conceptual design complete, all drawings finished
- EM Fabrication started, parts being machined
- Paralene foil specified, quote received
- Fit-check E-box provided to ESTEC
- Pin-pullers on order
- Prototype detector stack received; one coax broken in handling and repaired.
- Change from Triax to Coax between detectors and electronics in progress. New cable on order.
- EM and FM Magnets currently being assembled, delivery due 11-Nov-2002
- APL TAA signed
- No response yet on request to change requirement for 30keV ion threshold to 60keV
- First test of integrated detector/electronics assembly performed. Some noise issues to resolve
- Parts & Materials lists updated & submitted
- ESTEC PA plan waiting a response from project
- Structural analysis pending

Summary of ESTEC information obtained at status review:

- Analog and digital breadboards have been debugged (external contract, KTH) fully operational with GSE (interfaced with 1st release of the FPGA) at ESTEC since June 2002Functional and performance tests have been performed to validate the design
    - FPGA control & interfacing
    - Power supply switching
- Performance Tests:
    - Power consumption
    - Noise Level: typically 1100 erms (9.4keV FWHM) for 1 PDFE running alone
        - Tests being performed to identify noise sources with 2 PDFE board
- Integration Tests, Keil prototype detector with ESTEC breadboard
    - Fully operational instrument, no major changes for EM
    - Noise level isses to be worked
- Open Issues:
    - Power requirements; need more detail on noise level, may not need –5.1VA
- EM delivery to Kiel scheduled for 2nd week of January 2003
    - New layout by mid October
    - Second FPGA in test
    - New PDFE expected by March 2003
- Parts 80% in house
    - Testing/screening plans in work
    - Design has been re-worked to minimize number of part types

Caltech/JPL (SEP) Status
September 2002

4.1. *Summary of Status*

Activities centered on detector development, electronics development, and flight and GSE software development.

4.2. *Major Accomplishments:*

Detectors:

- The new holder for use in etching the L1 silicon detector wafers was tested prior to attempting to etch a wafer which had front-side L1 patterning. Following these successful tests, a detector wafer was etched. The only difficulty encountered was the etch-through of a small area that Micron Semiconductor had included at the edge of the wafer for test purposes. It is thought that this will not interfere with using the six L1 detectors areas. The etched wafer will be returned to Micron in early October so that they can complete the processing and test the resulting detectors.
- Micron has sent us several additional L1-patterned wafers, and we will start etching these in October.
- Micron has received detector mounts for several of the HET/LET detector designs from GSFC and is starting to install the silicon chips.

Electronics:

- PHASIC respin layout was submitted to AMIS for DRC check and a few minor DRC errors were found and corrected. The layout is ready and we are a few weeks ahead of our Oct.7 submission goal.
- Detailed design of the LET front end and MISC PCB level schematics are 95% complete. CAD schematics and PCB layout will follow soon.
- Consensus was reached regarding method of commanding SEP instruments: The IDPU will strip off the command headers prior to forwarding commands to SEP, and routing info will be contained in the command data stream itself. However, an open issue is how to encode the "hardware" reset commands to SEP. Dave Curtis has defined a single hardware reset command but we would like about 5 different ones (full boot from EEPROM banks A or B, SEP central only reboot from banks A or B, SEP central reboot over the serial command interface).
- Progress was made on issues relating to the SEPT ICD. Open issues remain: we would like to eliminate the "interrupt" line from SEPT and instead do periodic polling to handle their possible latch-up problem. They are going to let us know if this is adequate. They are also going to provide us with missing info regarding the timing of SEPT instrument responses.
- Pre-production review of the ceramic substrate for PHASIC hybrid performed by JPL and Teledyne personnel.
- Hybrid substrates are being made at Teledyne, due back in mid Oct.
- Finished layout of the PHASIC hybrid tester board and submitted it for fabrication.
- Worked on draft versions of ICDs between HET/LET/SIT/SEPT and SEP Central Electronics.
- Received flight EEPROM parts from Maxwell Technologies.
- Completed detailed design change of the bias supply to provide two independent power supplies, one for the positive voltages and one for the negative (SEPT Bias).

Prepared a layout of the new version of the bias supply, without the post regulators, and fabricated printed circuit boards.

- Changes were made in the design of the bias supply to allow proper operation when several detectors are shorted. Tests were performed to verify the design.
- Coordinating with procurement and changing drawings to comply with more readily available parts and package types.
- Updated schematics for analog/post-regulator board and for bias supply were sent to Caltech from Space Instruments.
- Resource update attached. Note the reduction in SEPT power and its harness mass. The first three pages show resource summary, while the following pages break down resource history.

Software:

- Worked on draft of SEP Commanding and User Manual.
- Continued software design activities for LET Flight Software.
- Began preparation of CDR materials.

GSE:

- Finished the CAMAC software and have started testing with a pulser, ADC card, and CAMAC input and output modules.
- Finished the documentation for the command communication interface between the SEP GSE and the telescope GSEs.

4.3. *Design Updates*

- Resource updates sent separately.

4.4. *Outstanding Problems*

- L1 thinning continues to be a challenge but new etching fixture has allowed the first thinning of a wafer to run to completion, a great step forward.

4.5. *New Problems*

- None.

4.6. *Top Risks.*

- The budget is very tight with no reserve being held at Caltech.
- Schedule slack that we show explicitly will be taken away from us.
- Development of the L1 detector. (See April and September reports for details.) Risk mitigated by creating slack in schedule and by starting a parallel development effort using different and more conventional manufacturing technique. New etching fixture works well and a thinned wafer will be sent to Micron in October for final processing into detectors.

4.7. *Problem/Failure Quick Look*

- None.

SIT MONTHLY TECHNICAL PROGRESS REPORT

September 2002

4.8. *SUMMARY of STATUS*

a. SIT TELESCOPE - Prototype is in house and working.
b. SIT TOF System - Flight unit 1 in house, tested in Germany, awaiting testing at UMd
c. SIT Energy/Logic System - Prototype energy system has been integrated with the prototype TOF system and both are under test with GSE logic board. Front end logic is being implemented at GSFC.
d. SIT HVPS - HVPS ETU working and at UMd

4.8.1. Schedule Changes

The current SIT schedule is available from Robert Palfy

4.9. *MAJOR ACCOMPLISHMENTS*

4.9.1. This Month

a. Energy/TOF - Thermal testing of the prototype energy and TOF systems was performed.
b. Logic - A beginning was made on laying out the EM logic board using the Yamaichi Actel socket. The socket part was generated and the schematic for the board was begun.
c. GSE: The Energy Bench Calibration program was completed and used in the thermal test of the system.
d. Reviews: Work was begun on preparing the draft CDR package due mid-October

4.9.2. Next Month

a. We expect to receive the engineering unit of the HVPS and to begin integrating it with the prototype telescope and the TOF and energy boards.
b. We will get Actel pinouts from George Winkert and will complete the layout of the EM logic board to support the front-end logic Actel chip.

4.10. *DESIGN UPDATES*

4.10.1. Resources

	Last Month	This Month	Change
Mass (g) *	1336	1336	0
Power (mW)**	1354	1354	0
Telemetry (bps)	418	418	0

* Includes 200g bookkept by GSFC for SIT structure

** Note: preliminary indications are that the HVPS power is higher than we have been carrying.
This will be reported next month when we test the EM HVPS at UMd.

4.11. *OUTSTANDING PROBLEMS*

4.12. *NEW PROBLEMS*

4.13. *NEW RISKS*

4.14. *PROBLEM/FAILURE QUICK LOOK*

Starts at first turn-on of flight hardware.

ID #	Description	Assignee	Opened	Closed

5. CESR (SWEA) Status

CESR- TOULOUSE- France **Author : Claude Aoustin / Project Manager**

SWEA PROGRESS REPORT # 13
(October 14, 2002)

September 2002

CESR is in charge of :

- Electrostatic analyzer with deflectors, grids and Retractable Cover
- Detector consisting of two MCP rings
- Amplifiers and discriminators
- 3 High voltages

5.1. *Summary of Status*

Mechanical design end 17/12/2001 completed
Mechanical analyzer fabrication end 22/04/2002 completed
Electronics fabrication completed, test completed
ETU Assembly completed 06/09/2002
Delivery to UCB was planned for 12/07/2002 : done 26/09/2002

5.2. *Major accomplishments*

Mechanical fabrication :

- First EM analyzer and housing fabricated.
- Deflector grids fabrication: one set (2 grids) fabricated. Transparency lower than expected (75% per grid). Could be increased for the flight models if necessary by having bigger cells.
- Verification under vacuum done 06/09/2002-24/09/2002 – MCP characterization – analyzer response – azimuthal resolution – deflector properties
- Electronics boards are designed, fabricated, populated and tested.
- Mechanical stand for the Pin Puller designed and fabricated for the EM2. It has been tested and presented on the 25/09/2002.
- A meeting with GSFC and NASA took place in CESR on the 25/09/2002 to verify the door mechanism and discuss the overall status of the experiment.

5.3. *Design Updates*

Mass : 1040 g (EM is 950g without cover opening mechanism)
Power : 446 mW min ; 662 mW max

5.4. *Outstanding Problems*

AMPTEKS amplifiers quality:
- additional burn in will be done : 1000h at 125°C on 10 pieces.
- under test at Hirex : subcontractor specialized for testing flight parts.

5.5. *New problems*

None

5.6. *Top Risks*

5.7. *Problem Failure Quick Look*

None

6. GSFC (MAG) Status

Nothing to report.

7. EPO at UCB

Monthly E/PO Report

September, 2002

Public Outreach:

- A traveling exhibit of NASA-sponsored art called "The Artistry of Space" was presented aboard the Artrain USA from September 5th to 8th , 2002 at the Richmond Field Station in Richmond, California. Along with the Center for Science Education at the Space Sciences Laboratory, IMPACT E/PO disseminated thousands of materials through the exhibit including the 3-D STEREO posters.
- Meetings were held to discuss the direction of E/PO projects for FY 03 and 04, using sounds created from HELIOS 1/2 data and future STEREO data. The concept of a museum kiosk with sounds and 3-D images was discussed. A website, "voices of space", is being transferred to the STEREO E/PO site which showcases sounds of the HELIOS mission and will be used for STEREO data. The website will include tutorials on space weather and making sounds from the satellite data.
- September 21st: STEREO educational materials were presented along with a lesson on sunspots for a professional development workshop for in-service high school science teachers. The workshop was organized by BAESI (Bay Area Earth Science Institute) and held on the campus of San Jose State University.
- A new E/PO scientist at the Center for Science Education joined our team. Bryan Mendez is a recent Doctoral Graduate of the UC Berkeley Astronomy Department and comes to us with great enthusiasm for Education and Public Outreach.

Respectfully Submitted,

STEREO/IMPACT E/PO scientists Nahide Craig and Bryan Mendez