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Subject: IMPACT Monthly Technical Progress Report, Contract NAS5-00133

Harry:

Enclosed is the monthly technical progress report for the STEREO IMPACT project for the month of August 2002.

Sincerely,

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CC:

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IMPACT Team

1. IMPACT Overview

This report is presented in sections by institution. Section 1 is an IMPACT Project Manager / System Engineer's overview.

1.1. *Contracting / Funding*

Funding to the end of FY02 is in place. Because of pipe-line delays in the system through to the subcontractors (Caltech and UMd) it is important that IMPACT be funded somewhat in advance of expected spending. *Since no FY03 funding is expected until a month or two into FY03, there may be difficulties in keeping work going.*

1.2. *Significant System-Level Accomplishments*

- Held peer reviews on IDPU/POCC and HET/SIT software.
- Participated in IMPACT I&T Telecon with APL/Project
- Participated in EMC & Contamination Committee telecons
- Participated in discussions with Project on deep dielectric discharge issues
- Decided on command exchange formats between different GSE and the POCC
- Worked with Project planner on integrated schedule.

1.3. *System Design Updates*

- None

1.4. *System Outstanding Issues*

- SEPT proton energy threshold not meeting requirement due to extra aluminum deposited to improve stray light rejection. Waiver submitted
- STE radiation source has not been approved yet by Project. Waiver submitted
- Operational heater power budget over allocation. Waiver to allocations submitted.

1.5. *Top 10 Risks*

Top 10 risks are attached. No change from last month.

IMPACT Top Ten Risks 4/2002

No.	Risk Item	Score	Mitigation	Mitigation Schedule						
				PDR	Bread-board Test	CDR	Sub-system Test	System Test	Env test	Early Orbit Test
UCB_5	IMPACT boom is a new design. Failure could affect Imager pointing requirements as well as boom-mounted instruments.	HIGH	Design for reliability. Early development and test to ensure reliability.	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH
UCB_21	Custom VLSI used in SEP may has schedule and cost risk	MEDIUM	Early development to prove design; use Amptek in place of VLSI in SIT (stll use VLSI in HET, LET); first run looks good, but a second run will be required	MEDIUM	MEDIUM	LOW	LOW	LOW	LOW	LOW
UCB_23	Non-standard parts qualification failure could impact delivery schedule	MEDIUM	Early parts selection and screening	MEDIUM	MEDIUM	LOW	LOW	LOW	LOW	LOW
UCB_15	GSFC Approval Requirements could delay instrument delivery or add cost	MEDIUM	Difficult to asses, history is mixed	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	LOW
UCB_4	The IDPU is a single point failure mechanisim for the IMPACT suite and PLASTIC	HIGH	IDPU is a simple, reliable system. Extra attention will be paid to ensuring its reliability	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH
UCB_13	IMPACT team is thin; loss of a critical team member could delay delivery	MEDIUM	Reassign work amongst team as and when required	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	LOW	LOW
UCB_11	Stringent EMI requirements may delay schedule if testing fails	MEDIUM	Careful design, early testing	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	LOW	LOW
UCB_1	ITAR restriction of information exchange with foreign CoIs may result in problems not discovered until late in the program	MEDIUM	Various channels of communication have been found within the ITAR restrictions to allow adequate information flow. Some exchanges are still forbidden and may cause a problem.	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	LOW
UCB_18	LET Detectors from a new manufacturer	MEDIUM	Backup L1 dtectors ordered; low risk, meet requirements	MEDIUM	MEDIUM	LOW	LOW	LOW	LOW	LOW
UCB_10	Complex Interlocking IMPACT schedule increases risk of late delivery to spacecraft	MEDIUM	A milestone schedule of deliveries has been set up to minimize schedule interaction and give power to control schedule to institutions while maintaining top level schedule slack; an integrated Project-level schedule is in progress. It is not clear yet if this will actually reduce risk.	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	LOW	LOW

2. Berkeley Status

2.1. *Summary of Status*

The UCB schedule with updated status will be delivered separately.

2.2. *Major Accomplishments*

SWEA/STE:

- SWEA/STE layout work complete, boards out to fab.
- SWEA/STE FPGA design / simulation test in progress.
- STE box/door ETU fab in progress.
    - Some design changes to lengthen the actuator wire per a recommendation from TiNi to limit stress.

IDPU:

- Data Controller Board ETU#1 configured for software development and interface testing.
- DCB ETU#2 delayed because of parts problem (UTMC RAM).
- Flight Software: Build #2: Tests in progress. Significant effort expended in ferreting out bugs in Spacecraft Emulator.
- Possible change of flight RAMs to ones with better SEU characteristics in negotiation with Project.

LVPS/HVPS:

- IDPU LVPS layout in progress (some changes from the peer review slowed things down a bit)
- SIT HVPS in test. Some problems with synchronization. Expect to deliver in September.

Boom:

- Thermal model delivered to APL. Some refinement of instrument models still in work
- Prototype tubes delivered and inspected. Meet ESC requirements
- Ring part designs adapted to as-built tubes; drawings in review. Expect to fab parts soon
- Joint thermal test delayed while glue is researched.
- Harness on order

GSE:

- C&T GSE delivered and tested with Emulator and ETU DCB. Some modifications in work to work around emulator problems
- SWEA/STE IDPU simulator GSE software in progress

2.3. *Design Updates*

2.4. *Outstanding Problems*

- Boom thermal issue; to be resolved by joint cold test
- UT80C196KD processor DMA problem needs to be resolved (pending DCB ETU #2 tests with new run processor)
- Boom schedule continues to slip

2.5. *New Problems*

- Need to resolve SRAM SEU issue

2.6. *Top Risks.*

No new risks identified.

2.7. *Problem/Failure Quick Look*

None.

3. GSFC (SEP) Status

STEREO/IMPACT/SEP/GSFC Progress Report for August, 2002 – (von Rosenvinge, Baker, Hawk, Reames, Shuman, Wortman)

3.1. *Summary of Status*

Mostly on-schedule. Four HET H3 and ten LET L1 detector mounts have been sent to Colin Wilburn at Micron. The LET L2 and LET L3 detector mounts are currently being manufactured together with redos of the L1 and H1 mounts. The PCB coupons and mounts for the H3 detectors have all passed inspection. The remaining mechanical effort has been on the mechanical design of the HET telescope and its electronics board.

3.2. *Major Accomplishments*

The HET and SIT Software Requirements and Software Design Review took place on August 22. We have made good progress on our software. A problem has been identified with the prototype Caltech ASIC test setup that was initially thought to be software related. It now appears that there may be a hardware problem, but this has not been as yet determined.

3.2.1. Next month-

- Continue work on the overall SEP mechanical design, including the SIT door.
- Continue work on the HET GSE, on-board software, and PHA ASIC test software.
- Complete testing the PHA ASIC. This requires fixing the problem alluded to above.
- Complete the front-end ASIC design for SIT.
- Prepare for the CDR in November.

3.3. *Design Updates*

None quantified this month.

3.4. *Outstanding Problems*

No major problems outstanding.

3.5. *New Problems*

None.

3.6. *Top Risks*

No significant risks at GSFC? Need to ensure that manpower becomes available per the current plan.

3.7. *Problem/Failure Quick Look*

4. Kiel (SEPT) Status

SEPT Monthly Technical Progress Report
August 2002

4.1. *Summary of Status*

1. The first test of the integrated detector/electronics assembly was finally performed with satisfying results.
2. A SEPT Team Meeting was held at ESTEC, which helped to acquaint the new staff (Stephan Boettcher, Ludovic Duvet) with the members of the team, clarify misunderstandings, resolve TBD's, revise documents, and identify urgent actions.
3. Fabrication of mechanical parts for Engineering Model (EM) Sensor and E-box delayed by 2 months, partly by overload in mechanical workshop during vacation season, partly by late design changes. Revised schedule reflects these changes. No impact on flight model fabrication so far.
4. Fabrication of new set of boards (analogue and digital) with new version of FPGA.
5. PA plan Rev. 2 released.

4.2. *Major Accomplishments*

1. From August 26 – 28, the protoptype detector stack was integrated for the first time ever with a new set of prototype boards of the analogue and digital electronics. The first SEPT electron spectrum has been recorded using a Bi207 radioactive source with conversion electron lines at 482, 565, 975 and 1060 keV in vacuum. This test is considered a success, although the noise background was not yet satisfactory: a trigger threshold of 80 keV was used, the goal is 20 keV. Further layout changes, shielding and grounding studies need to be performed to improve the background noise level.
2. The EGSE performed nicely during these tests, improvements for more comfort and extended functionality were identified. This is mostly a software task, but also new hardware is envisaged for a dedicated LVPS and bias supply simulator.
3. The design of the electronics for EM is about to be closed (pending noise study outcome). Agreement was reached with Branislav on J2 connector pin-out.
4. Parts and material lists have been finalized and will be released in September. SEPT schedule is updated and will be released in September. Percentage progress will be implemented in the future. PA Plan Rev. 2 has been released, no comments received so far.
5. Parts procurement is in good shape: numerous flight components have been received, including the FPGA.

4.3. *Design Updates*

4.4. *Outstanding Problems*

4.5. *New Problems*

1. Thermal hardware needs to be specified: operational heater, survival heater, harness routing, J1 connector.
2. Who is responsible for developing and implementing the various components of

thermal hardware including silvered quartz second surface mirrors (SSM, if needed), MLI and thermal paint?

4.6. *Top Risks*

4.7. *Problem/Failure Quick Look*

5. Caltech/JPL (SEP) Status

August 2002

5.1. *Summary of Status*

Activities centered on detector development, electronics development, and flight and GSE software development.

Major Accomplishments:

Detectors:

- The L1 wafer etching that was in progress near the end of June failed when the front (ion-implanted) surface of the wafer (which is supposed to be protected from the KOH etchant) was attacked along the boundaries of the active areas. A conference call and several emails between JPL, Caltech, and Micron Semiconductor led to the realization that the points where the front surface was being attacked correspond to boundaries between areas that do and do not have a relatively thick (approximately 0.9 micron) oxide layer on top of the silicon. It is now thought the failures are attributable to the fact that the chromium and gold evaporations used to protect this surface of the detector are thinner than this step and are probably unable to prevent the KOH from getting to the silicon along this boundary.
- To solve the front-side etching problem a new wafer holder was designed for use in the etching. If this holder performs as designed, it should completely prevent KOH from coming in contact with the front of the detector. Fabrication of the holder has been completed and it will be tested in early September with some silicon wafers that do not have detector implants prior to resuming the etching of the actual detector wafers. JPL presently has two of these detector wafers that can be etched as soon as the wafer holder has been successfully tested, and Micron reports that they have three more that can be shipped when needed.
- Thickness maps were made of two of the 3-inch diameter x 20-micron thick wafers that Micron had purchased for fabrication of the "plan B" L1 detectors. A portion of the area was found to have thickness and thickness uniformity suitable for meeting LET requirements. However there was a sizeable variation of both parameters on each wafer, so it may be necessary to reject some detectors based on thickness measurements that we will make after the detectors have been fabricated.
- Micron has received from GSFC the mounts for prototype L1 and H3 detectors. They expect to be mounting some detectors of each type in September.

Electronics:

- Mods to PHA chip design and layout were completed and the layout was checked versus the new schematic using our automated tools. The chip is ready for co-submission with the "handheld" chip, which is nearly complete. Co-submission will probably occur ahead of the Oct. 7 goal.
- The electrical design of the test fixture for the PHA hybrid was done and CAD schematics and layout are in process.
- The detailed electrical design of the LET front end and MISC boards was started.
- The layout of the PHA hybrid substrate was completed at JPL on schedule by Aug. 9. The purchase order for substrate manufacturing is expected to be placed in September.

- The initial draft of the HET-SEP central ICD went out and is being iterated.
- Radiation total dose testing of the PHA chip occurred at Aerospace Corp. in early August. Three parts were exposed. One worked fine after 8 Krads, but failed after an additional 12 Krads (20 Krad total). Another worked fine after 12 Krads. And another worked after 8 Krads (the mission requirement). The dose rate was high at 50 rad/sec using Co60. The threshold shift for nmos and pmos transistors was only -200 uV/Krad and -360 uV/Krad respectively, so the part failure at 20 Krad could not be attributed to threshold shifts. We will redo the total dose test after the respin and take a closer look at whether the environments in LET and HET provide adequate shielding. When we redo the dose test we will include runs at a lower dose rate.
- Automated testing of the PHA chips was done to characterize the chips pre and post radiation. With refinement, the automated test routines will carry over to hybrid testing later.
- The PHA chip was operated at high event rates and as expected no significant increase in power consumption occurred. We will check again later at the board level. Power fluctuation with event rate is expected to be dominated by variation in the MISC power of about ±20%.
- New schedule and tracking of our electrical manpower has spurred progress and demonstrated the need to focus key personnel on STEREO, while off loading certain non-STEREO tasks to outside vendors.
- Provided flight parts list for LET/SEP Central Electronics to GSFC parts specialist, Antonio Reyes and UCB's Ron Jackson for review.
- Space Instruments continued detailed design of the Bias Supply and Analog/Post-Reg Boards.
- Provided schematic and parts list for +5VRef circuit, -5Vref circuit, and heater on/off circuit.
- Completed tests of the proof of concept Bias Supply and evaluated the test results. Now we are in the process of updating the Bias Supply Design to further reduce power consumption and required volume. Detailed design of the modified version is completed. Tests on new proof of concept board are completed and results show lower power consumption.
- Design has been modified again to make two totally independent power supplies, one for the positive and another for the negative voltages. Schematic and parts list for the new design are completed.

Software:

- Wrote draft of LET Level 1 Data Format Document.
- Continued software design activities for LET Flight Software

GSE:

- Wrote the low-level software for getting data from the Varian multi-gauge controller. A small amount of higher-level software remains to be written.
- Wrote the lowest-level routines for using the serial IEEE-488 controller, which is used to interface the CAMAC crate. The higher-level software for using the IEEE-488 controller to access the data from the CAMAC modules in the crate remains to be written.

- Developed and received consensus on the high-level details of the command communication interface to be used among the SEP GSE, the telescope GSEs of the SEP instrument suite, and the IMPACT GSE.
- Started to work out the lower-level details of the command communication interface to be used among the SEP GSE, the telescope GSEs, and the IMPACT GSE and began writing documentation that details the command communication interface.
- Attended the HET Software Review by phone.

5.2. *Design Updates*

- No resource updates this month.

5.3. *Outstanding Problems*

- L1 thinning continues to be a challenge.

5.4. *New Problems*

- None.

5.5. *Top Risks.*

- The budget is very tight with no reserve being held at Caltech.
- Schedule slack that we show explicitly will be taken away from us.
- Development of the L1 detector. (See April and September reports for details.) Risk mitigated by creating slack in schedule and by starting a parallel development effort using different and more conventional manufacturing technique.
- Development of the VLSI chip. (See September report for details.) Risk mitigated by providing for two more months for the layout and checking while still keeping 30 weeks for a second run which now will be necessary. We anticipate submitting the second VLSI run in early October 2002.

5.6. *Problem/Failure Quick Look*

- None.

6. SIT MONTHLY TECHNICAL PROGRESS REPORT

6.1. *SUMMARY of STATUS*

a. SIT TELESCOPE - Prototype is in house and working.
b. SIT TOF System - Flight unit 1 in house, tested in Germany, awaiting testing at UMd
c. SIT Energy/Logic System - Prototype energy system has been integrated with the prototype TOF system and both are under test with GSE logic board. Front end logic is being implemented at GSFC.
d. SIT HVPS - HVPS ETU fabrication in process

6.1.1. Schedule Changes

The SIT schedule has been updated and is available from Robert Palfy

6.2. *MAJOR ACCOMPLISHMENTS*

6.2.1. This Month

Energy/TOF - The newly laid out energy PC board was received. Waiting for parts to assemble.

Logic - Working with George Winkert at GSFC, it was decided that progress on implementing and checking the front end logic could best be made by decoupling the development of the logic from that of the MISC. Accordingly it was agreed that George will generate the front-end logic on an EM Actel without waiting for the MISC and its software. UMd will fabricate an EM logic board to connect this chip to the remaining SIT components and to the SIT GSE computer which will stand in for the MISC, as it does now with the breadboard (Xilinx) logic. Testing and modification of the front-end logic can then proceed independently of the MISC effort. This testing is expected to begin in late September/early October.

GSE: The GSE LVPS was completed and calibrated and monitor software was written to allow the GSE to be aware of the voltages and currents consumed by the SIT electronics. The Energy Bench Calibration program was completed and is undergoing test.

Reviews - We supported the SEP Flight Software Peer Review at GSFC.

6.2.2. Next Month

We will perform thermal testing of the prototype energy and TOF systems.

We expect to receive the engineering unit of the HVPS and to begin integrating it with the prototype telescope and the TOF and energy boards.

We will layout the EM logic board to support the front-end logic Actel chip.

6.3. *DESIGN UPDATES*

6.3.1. Resources

	Last Month	This Month	Change
Mass (g) *	1336	1336	0
Power (mW)	1354	1354	0
Telemetry (bps)	418	418	0

* Includes 200g bookkept by GSFC for SIT structure

6.4. *OUTSTANDING PROBLEMS*

6.5. *NEW PROBLEMS*

6.6. *NEW RISKS*

6.7. *PROBLEM/FAILURE QUICK LOOK*

Starts at first turn-on of flight hardware.

ID #	Description	Assignee	Opened	Closed

7. CESR (SWEA) Status

CESR- TOULOUSE- France **Author : Claude Aoustin / Project Manager**

SWEA PROGRESS REPORT # 12
(September 16, 2002)

August 2002

CESR is in charge of :
- Electrostatic analyzer with deflectors, grids and Retractable Cover
- Detector consisting of two MCP rings
- Amplifiers and discriminators
- 3 High voltages

7.1. *Summary of Status*

Due to the vacation period in France in August, few progress done during this month !
Mechanical design end 17/12/2001 completed
Mechanical analyzer fabrication end 22/04/2002
completed
Electronics fabrication completed, test completed
ETU Assembly start 17/06/2002 was planned end 07/2002 will be end 08/2002
Delivery to UCB was planned for 12/07/2002 : will be end September

7.2. *Major accomplishments*

Mechanical fabrication :
- First EM analyzer and housing fabricated.
- Deflector grids fabrication: one set (2 grids) fabricated. Transparency lower than expected (75% per grid). Could be increased for the flight models if necessary by having bigger cells.
- Spheres treatment and black coating finished. Spheres received in Toulouse.
- Verification under vacuum in September. Vacuum chamber ready, Electron beam tested before verification of the instrument at some keV.
- Electronics boards are designed, fabricated, populated and tested.
- Next step is the integration of the MCP. All mechanical parts fabricated.
- Some delay on the MCP integration due to the late delivery of the MCP stands (gilded rings). Done beginning of September.
- Mechanical stand for the Pin Puller designed and fabricated for the EM2.

7.3. *Design Updates*

Mass : 1040 g
Power : 446 mW min ; 662 mW max

7.4. *Outstanding Problems*

AMPTEKS amplifiers quality:
- additional burn in will be done : 1000h at 125°C on 10 pieces.
- under test at Hirex : subcontractor specialized for testing flight parts.

7.5. *New problems*

None

7.6. *Top Risks*

7.7. *Problem Failure Quick Look*

None

8. GSFC (MAG) Status

Nothing to report.

9. EPO at UCB

August E/PO Report:

We are looking into sonorization of future STEREO data. A programmer has made a good progress with 'test-data' using Helios1/2 data, ands we are proceeding with a Music Professor at UCB's The Center for New Music and Audio Technologies to investigate further this project.

The Abstract below is submitted to the AGU Fall 2002 Meeting, highlighting the Mission Scientists (J. Luhmann) and EPO (N. Craig) collaboration with

Participation of our Programmer and Science Museum Collaborator.

High "IMPACT" STEREO EPO: Exploiting Opportunities for High Visibility Activities On a Shoestring

N. Craig, J.G. Luhmann, I. Sircar (UC Berkeley Space Sciences Laboratory) and
N. Wittman (Exploratorium)

Our dynamic Sun offers exciting opportunities to share research discoveries of NASA's Sun Earth Connection Missions for the pre-college education and public outreach communities. NASA's STEREO/IMPACT Mission E/PO seeks to offer national programs for broad audiences that highlight the Mission's solar and geo-space activities. The partnership between the Mission scientist and the Mission E/PO is essential to fully reap the fruits of this rich education and public outreach effort. We will share two events, a high visibility, successful Eclipse 2001 participation and a new project – an exciting prototype program converting the science results of solar energetic particle data to sound, and ultimately to create a composition inspired by these sounds and related solar images by a musician. Data from an earlier twin-spacecraft Mission, Helios1/2 (courtesy of D. Reames, GSFC and the Helios mission investigators) are used as a testbed for creating the stereo sounds from the future STEREO data. We hope these efforts will lead to a recording by an ensemble as well. We will discuss lessons learned and future opportunities for scientist participation.