Harry Culver, Code 740.1
STEREO IMPACT Instrument Manager
Goddard Space Flight Center
Greenbelt, MD. 20771

Subject: IMPACT Monthly Technical Progress Report, Contract NAS5-00133

Harry:

Enclosed is the monthly technical progress report for the STEREO IMPACT project for the month of July 2002.

Sincerely,

David Curtis
IMPACT Project Manager
University of California, Berkeley

CC:

Julie.A.Janus.1@gsfc.nasa.gov
Claudia.Krogel.1@gsfc.nasa.gov
Harry.Culver@gsfc.nasa.gov
IMPACT Team

1. IMPACT Overview

This report is presented in sections by institution. Section 1 is an IMPACT Project Manager / System Engineer's overview.

1.1. *Contracting / Funding*

Funding to the end of FY02 is almost in place. Because of pipe-line delays in the system through to the subcontractors (Caltech and UMd) it is important that IMPACT be funded somewhat in advance of expected spending.

1.2. *Significant System-Level Accomplishments*

- Completed IMPACT power converter ICD
- Held peer reviews on power converters and STE door mechanisim.
- Held a team telecon to work out data analysis plans
- Participated in Contamination Committee telecon
- Worked on Actel common buy. Contractual problems working it though UCB; GSFC to look into making the buy.
- Decision was made not to support the SWAVES aircoil on the IMPACT boom.
- Worked with Project planner on integrated schedule.

1.3. *System Design Updates*

- None

1.4. *System Outstanding Issues*

- SEPT proton energy threshold not meeting requirement due to extra aluminum deposited to improve stray light rejection. Waiver submitted
- STE radiation source has not been approved yet by Project. Waiver submitted
- Operational heater power budget over allocation. Waiver to allocations submitted.

1.5. *Top 10 Risks*

Top 10 risks are attached. No change from last month.

IMPACT Top Ten Risks 4/2002

No.	Risk Item	Score	Mitigation	Mitigation Schedule						
				PDR	Bread-board Test	CDR	Sub-system Test	System Test	Env test	Early Orbit Test
UCB_5	IMPACT boom is a new design. Failure could affect Imager pointing requirements as well as boom-mounted instruments.	HIGH	Design for reliability. Early development and test to ensure reliability.	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH
UCB_21	Custom VLSI used in SEP may has schedule and cost risk	MEDIUM	Early development to prove design; use Amptek in place of VLSI in SIT (stll use VLSI in HET, LET); first run looks good, but a second run will be required	MEDIUM	MEDIUM	LOW	LOW	LOW	LOW	LOW
UCB_23	Non-standard parts qualification failure could impact delivery schedule	MEDIUM	Early parts selection and screening	MEDIUM	MEDIUM	LOW	LOW	LOW	LOW	LOW
UCB_15	GSFC Approval Requirements could delay instrument delivery or add cost	MEDIUM	Difficult to asses, history is mixed	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	LOW
UCB_4	The IDPU is a single point failure mechanisim for the IMPACT suite and PLASTIC	HIGH	IDPU is a simple, reliable system. Extra attention will be paid to ensuring its reliability	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH
UCB_13	IMPACT team is thin; loss of a critical team member could delay delivery	MEDIUM	Reassign work amongst team as and when required	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	LOW	LOW
UCB_11	Stringent EMI requirements may delay schedule if testing fails	MEDIUM	Careful design, early testing	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	LOW	LOW
UCB_1	ITAR restriction of information exchange with foreign CoIs may result in problems not discovered until late in the program	MEDIUM	Various channels of communication have been found within the ITAR restrictions to allow adequate information flow. Some exchanges are still forbidden and may cause a problem.	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	LOW
UCB_18	LET Detectors from a new manufacturer	MEDIUM	Backup L1 dtectors ordered; low risk, meet requirements	MEDIUM	MEDIUM	LOW	LOW	LOW	LOW	LOW
UCB_10	Complex Interlocking IMPACT schedule increases risk of late delivery to spacecraft	MEDIUM	A milestone schedule of deliveries has been set up to minimize schedule interaction and give power to control schedule to institutions while maintaining top level schedule slack; an integrated Project-level schedule is in progress. It is not clear yet if this will actually reduce risk.	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	LOW	LOW

2. Berkeley Status

2.1. *Summary of Status*

The UCB schedule with updated status will be delivered separately.

2.2. *Major Accomplishments*

SWEA/STE:

- Pulse reset glitch problems resolved.
- SWEA/STE layout work in progress. First board done (DAC board), but waiting remaining boards before release. Detector board layout complete.
- SWEA/STE FPGA design in progress.
- STE door peer review completed. STE box/door ETU fab in progress.

IDPU:

- Data Controller Board ETU#1 testing complete, delivered to software development.
    - Problems with the UT80CRH196KD DMA facility. Received a prototype of UTMC new part that is supposed to fix this, mounted in ETU DCB #2. We also have a work-around that we will use if necessary. Currently using the work-around.
- DCB ETU#2 delayed because of parts problem (UTMC RAM).
- Flight Software: Build #1 (ETU test) complete) Build #2: Add STE code. Start testing
- IDPU ETU box fabrication complete. Fit-check with DCB OK.

LVPS/HVPS:

- Power converter peer review completed.
- IDPU LVPS layout in progress (some changes from the peer review slowed things down a bit)
- SIT HVPS in fabrication.
- LVPS/HVPS ICD complete

Boom:

- Thermal model delivered to APL. Some refinement of instrument models still required.
- Prototype /Flight tubes on order.
- Working on parts drawings. Expect to place ring orders mid August.
- Added fasteners to joint design to back-up glue
- Joint thermal test planned for mid August
- Harness sent out to quote

GSE:

- MAG IDPU simulator software/hardware delivered to GSFC
- Work for C&T GSE in progress (Command encoder, MOC Interface).
- Second spacecraft emulator received from APL (currently one at Elf, one at UCB). Working out communication issues between emulator & C&T GSE.

2.3. *Design Updates*

2.4. *Outstanding Problems*

- Boom thermal issue; to be resolved by joint cold test
- UT80C196KD processor DMA problem needs to be resolved

2.5. *New Problems*

2.6. *Top Risks.*

No new risks identified.

2.7. *Problem/Failure Quick Look*

None.

3. GSFC (SEP) Status

STEREO/IMPACT/SEP/GSFC Progress Report for July, 2002 – (von Rosenvinge, Baker, Hawk, Reames, Shuman, Wortman)

3.1. *Summary of Status*

Mostly on-schedule. The HET H3 detector mounts have been received and are undergoing inspection. The LET2 and LET3 detector mounts designs have been approved and sent out for bids. The HET H1 detector mounts which we received did not meet specifications and so have been resubmitted for fabrication. The L1 and H3 connectors have been received. The PCB coupons and mounts for the H3 detectors have been sent to inspection. The design configuration for the SEP Low Voltage Power Supply was updated.

3.2. *Major Accomplishments*

Some problems have been identified with the prototype Caltech ASIC test software and are in the process of being fixed. So far, tests of the ASIC have proved the chip to work extremely well.

George Winkert completed a wire list for the SIT front-end logic on schedule.

The HET Software Requirements Review was expanded to include software design and was rescheduled for August 22.

Delivered a thermal model to APL.

3.2.1. Next month

- Fabricate the H1, L2, and L3 detector mounts. Continue work on the overall SEP mechanical design.
- Conduct Software Requirements Review on August 22.
- Continue work on the HET GSE, on-board software, and PHA ASIC test software.
- Complete testing the PHA ASIC.
- George Winkert to meet with Peter Walpole concerning the preliminary front-end electronics design for SIT.

3.3. *Design Updates*

None quantified this month.

3.4. *Outstanding Problems*

No major problems outstanding.

3.5. *New Problems*

None.

3.6. *Top Risks*

No significant risks at GSFC? Need to ensure that manpower becomes available per the current plan.

3.7. *Problem/Failure Quick Look*

4. Kiel (SEPT) Status

SEPT Monthly Technical Progress Report
July 2002

4.1. *Summary of Status*

- July is vacation month. No much progress to report.
- Damaged detector stack repaired at Canberra Company. The test of the integrated detector/electronics assembly is scheduled for August, 2002.
- Specification for coax cables and connectors issued. Quotation not yet received. Cables are urgently needed for assembly of flight detector stacks.
- Monte Carlo simulation refined.
- New project manager at ESTEC, Ludovic Duvet, started working on July 1, 100 % of his time for SEPT.
- Continued noise investigation in analogue electronics.

4.2. *Major Accomplishments*

1. The first mechanical parts of the ETU and FM's are machined: rings for assembly of the Parylene foils. They will need to undergo surface treatment (Alodine 1200) before being sent to the foil manufacturer.
2. The coax inner lead of one of the cables of the detector (lab model) was broken inside the detector mount due to undue bending just outside of the mount, possibly corroborated by poor stripping. The soldering was Okay. Both the procedure for cable stripping and the test bracket design for holding the detector housing with cables will be revised to avoid this problem for ETU and FM's.
3. The recent change from triax to coax cables and connectors makes a new specification necessary (the triax cable was already ordered and delivered). Companies are contacted, quotation not yet received.
4. The mathematical model was refined to reconstruct input spectra from the SEPT histograms.
5. The new ESTEC project manager started his work for SEPT. Using surplus detectors from our SOHO instrument, which have similar detector characteristics, investigations are going on to cope with the noise level in the analogue electronics.

4.3. *Design Updates*

4.4. *Outstanding Problems*

4.5. *New Problems*

4.6. *Top Risks*

4.7. *Problem/Failure Quick Look*

5. Caltech/JPL (SEP) Status

July 2002

5.1. *Summary of Status*

Activities centered on detector development, electronics development, and GSE software development.

Major Accomplishments:

Detectors:

- During the thinning of the silicon wafer containing six copies of the L1 detector with the front (junction) side (started in June) it was observed that the evaporated gold coating on the front side was being attacked by the KOH etchant in regions along the boundaries between the active segments. This explains the previously-observed problem where the silicon etched through between the ion-implanted segments. In that case the gold must have etched all the way through allowing the KOH to attack the silicon. On the present wafer, etching of the gold was noticed and we were able to evaporate additional gold onto the wafer before proceeding. At the end of July the etch was progressing.
- At Micron Semiconductor, work continued on the 20 micron wafers for the "plan B" L1 detectors. Ion implantation was done on the front (junction) side of several wafers.
- Two of the 20-micron, 3-inch-diameter wafers were received (unprocessed) from Micron. The thickness uniformity of these wafers will be evaluated at Caltech in August.
- At JPL, improvements were made in the vacuum system for alpha-particle testing of the L1 detectors. We are now achieving the design vacuum of 10^-6 torr.
- Micron's work on the prototype L2, L3, H1, and H3 detectors remains on hold waiting for receipt of detector mounts.
- Detector Development System - After a four-month hiatus, started work on the software for getting data from the Varian Multi-Gauge Controller and the CAMAC crate. System testing with radiation sources should begin in early September.

Electronics:

- Assembled and tested hardware in preparation for upcoming radiation tests (latch-up and total dose) of the VLSI chip. Latch-up test done at end of July showed no latch-up up to 80 MeV/mg/cm2.
- Made design changes for the PHA chip respin and finalized changes.
- Reviewed system design issues. Adopted final sensor to SEP central interface designs after SPICE simulation of performance. Decided to move analog ±5V regulators and precision 5V reference to individual LET and HET sensors pending availability of layout room. Updated LET and HET power interface to have ±6 volts rather than ±5 volts. Increased HET and LET digital power supply voltages by 0.1 volts to account for local filter drop. ICDs in progress.
- Finalized selection and procurement of discrete parts for the VLSI hybrid and started the final layout phase of the ceramic substrate for the hybrid.

- Obtained a quote for flight clock oscillators from Q-Tech in accordance with Level 2 requirements.
- Received schematics from Space Instruments for +5V analog regulator and -5V reference generator, which will be situated locally on LET and HET detector boards. We also received preliminary designs for the Analog/Post-Regulator and Bias Supply boards, along with their power and mass estimates.
- Started formal work on electrical ICDs between the individual sensors and SEP Central Electronics.
- Received preliminary flight parts list for SEP LVPS and included it in the parts list for LET/SEP Central Electronics, which will be sent to GSFC parts specialist, Antonio Reyes, and UCB's Ron Jackson for review.
- Resource tables (to be submitted separately) reflect mass and power updates.

GSE:

- In the first part of the month, continued work on the Graphical User Interface (GUI) code for handling the page display windows for LET. This is Java code that creates and manages the windows, which will contain the LET page displays and responses to the user's mouse and keyboard inputs. This code is independent of the data format. In the latter part of the month, this work was set aside in favor of next item.
- Started work on defining the commanding requirements for the SEP GSE software. In July, developed a strawman proposal for commanding while SEP is at Caltech and circulated the proposal internal to Caltech. Next month, a modified proposal covering SEP commanding for all SEP activities, except the end-to-end test at the accelerator, will be distributed team-wide.
- Worked on software to control GPIB instruments and serial ports for VLSI testing and software to automate VLSI testing during total dose tests.

5.2. *Design Updates*

- Mass and power estimates will be provided separately.

5.3. *Outstanding Problems*

- L1 thinning continues to be a challenge.

5.4. *New Problems*

- None.

5.5. *Top Risks.*

- The budget is very tight with no reserve being held at Caltech.
- Schedule slack that we show explicitly will be taken away from us.
- Development of the L1 detector. (See April and September reports for details.) Risk mitigated by creating slack in schedule and by starting a parallel development effort using different and more conventional manufacturing technique.
- Development of the VLSI chip. (See September report for details.) Risk mitigated by providing for two more months for the layout and checking while still keeping 30 weeks for a second run which now will be necessary. We anticipate submitting the second VLSI run in early October 2002.

5.6. ***Problem/Failure Quick Look***

- None.

6. SIT MONTHLY TECHNICAL PROGRESS REPORT

July 2002

6.1. *SUMMARY of STATUS*

a. SIT TELESCOPE - Prototype is in house and working.
b. SIT TOF System - Flight assembly complete and testing in progress
c. SIT Energy/Logic System - Prototype energy system has been integrated with the prototype TOF system and both are under test with GSE logic board
d. SIT HVPS - HVPS ETU fabrication in process

6.1.1. Schedule Changes

The SIT schedule has been updated and is available from Robert Palfy

6.2. *MAJOR ACCOMPLISHMENTS*

6.2.1. This Month

Energy/TOF - The energy and TOF prototype boards were stacked in a fixture and checked. Results were good: no new interferences were discovered. Flight TOF boards were assembled and testing was begun.
A new prototype energy PC board layout was generated and sent out for fabrication. This layout incorporates the changes made getting the original design to work, decals for the flatpack version of the A275 hybrids, and corrected board size and board stacking details.

GSE: A GSE LVPS was designed and the PC board was laid out and procured. When complete this supply will provide regulated LV to the SIT electronics with voltages and currents monitored. A bench calibration LabView program was begun. When complete this program will allow us to perform automated bench calibrations on the SIT electronics.

6.2.2. Next Month

We expect the flight TOF boards to be shipped in early August.

We expect to complete the GSE LVPS and bench calibration program and to perform thermal testing on the prototype TOF.

We expect to receive the engineering unit of the HVPS and to begin integrating it with the prototype telescope and the TOF and energy boards.

6.3. *DESIGN UPDATES*

6.3.1. Resources

	Last Month	This Month	Change
Mass (g) *	1336	1336	0
Power (mW)	1354	1354	0
Telemetry (bps)	418	418	0

* Includes 200g bookkept by GSFC for SIT structure

6.4. *OUTSTANDING PROBLEMS*

6.5. *NEW PROBLEMS*

6.6. *NEW RISKS*

6.7. *PROBLEM/FAILURE QUICK LOOK*

Starts at first turn-on of flight hardware.

ID #	Description	Assignee	Opened	Closed

7. CESR (SWEA) Status

CESR- TOULOUSE- France **Author : Claude Aoustin / Project Manager**

SWEA PROGRESS REPORT # 11

(August 15, 2002)

July 2002

CESR is in charge of :

- Electrostatic analyzer with deflectors, grids and Retractable Cover
- Detector consisting of two MCP rings
- Amplifiers and discriminators
- 3 High voltages

7.1. *Summary of Status*

Mechanical design end 17/12/2001	completed
Mechanical analyzer fabrication end 22/04/2002	completed
Electronics fabrication	completed
Test	completed
ETU Assembly start 17/06/2002	was planned end 07/2002 will be end 08/2002
Delivery to UCB was planned for 12/07/2002 :	not before mid September !

7.2. *Major accomplishments*

Mechanical fabrication :

- First EM analyzer and housing fabricated.
- Deflector grids fabrication: one set (2 grids) fabricated. Transparency lower than expected (75% per grid). Could be increased for the flight models if necessary by having bigger cells.
- Spheres treatment and black coating finished. Spheres received in Toulouse.
- Verification under vacuum in September. Vacuum chamber ready, Electron beam tested before verification of the instrument at some keV.

Electronics boards are designed, fabricated, populated and tested.
Next step is the integration of the MCP. All mechanical parts fabricated.
Will be done end August.

Pin Puller arrived in Toulouse. Given to the subcontractor. Mechanical support designed and under fabrication for the EM2.

7.3. *Design Updates*

Mass : 1040 g
Power : 446 mW min ; 662 mW max

7.4. *Outstanding Problems*

AMPTEKS amplifiers quality:
- additional burn in will be done : 1000h at 125°C on 10 pieces.
- specification given to Hirex : subcontractor specialized for testing flight parts.

7.5. N*ew problems*

None

7.6. *Top Risks*

7.7. *Problem Failure Quick Look*

None

8. GSFC (MAG) Status

Nothing to report.

9. EPO at UCB

EPO for JULY Report: Outreach to various summer school programs:-100 students got introduced to STEREO/IMPACT

"*Our very Own Star: the Sun*" and its Spanish Version *" Nuestra PropiaEstrella*: *el Sol*" books were distributed to the 30 3rd graders of each of Vannoy Elementary School of Castro Valley, CA and the Washington School of Richmond, CA. The EPO lead Nahide Craig participated also in the classroom talk about the Sun and space weather at Washington School in July 26th in Richmond. This program is part of the Academic Talent Development Program of UC Berkeley and it is conducting 5-week summer science program focusing on the "Active Sun". In July 31st, 30 students grade 1st through 5th visited SSL from the Prospect Sierra School of El Cerrito CA and "observed the active sun" with 'Sunspotters" and received the "The Sun" books. The STEREO Missions goals and the "STEREO" effect were also discussed as relevant to elementary students as possible and the 'FUN" demonstration of looking at the STEREO poster with the 3-D glasses received very well by the students.

Respectfully Submitted.

Nahide Craig