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Subject: IMPACT Monthly Technical Progress Report, Contract NAS5-00133

Harry:

Enclosed is the monthly technical progress report for the STEREO IMPACT project for the month of May 2002.

Sincerely,

David Curtis
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CC:

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IMPACT Team

1. IMPACT Overview

This report is presented in sections by institution. Section 1 is an IMPACT Project Manager / System Engineer's overview.

1.1. *Contracting / Funding*

The current allotment should run out around the end of June, so a new allotment is needed soon. Because of pipe-line delays in the system through to the subcontractors (Caltech and UMd) it is important that IMPACT be funded somewhat in advance of expected spending (at this time we have funded UMd through the end of FY02).

We expect NASA to sign up to the new budget corresponding to the launch slip shortly.

1.2. *Significant System-Level Accomplishments*

- Working EMC issues; all waivers but one approved; the last has no concerns.
- First monthly IMPACT/PLASTIC telecon to discuss issues (mostly IDPU software).
- IMPACT Configuration Management Plan has been agreed on.
- PAIP: Working the ESTEC appendix (the last hurdle). Project comments to the latest version have been forwarded to ESTEC.
- Worked with Project planner on integrated schedule
- Worked with APL on thruster contamination/heating issues
- Completed SEP Central/LET Software Requirements Review at Caltech
- Still working on parts screening issues (selecting contractors, developing details test specs), getting approvals.

1.3. *System Design Updates*

- Change in location of STE-U under consideration to alleviate space issues at sunny end of boom (working with APL).
- Addition of STE calibration sources (working with Project on approvals)

1.4. *System Outstanding Issues*

- ESD issues with sun-facing surfaces (ITO contamination issue vs Goddard Composite Coating). Working with APL & Project to find a solution that meets ESC, thermal, contamination requirements.
- SEPT proton energy threshold not meeting requirement due to extra aluminum deposited to improve stray light rejection
- Data Analysis meeting to outline Data Analysis Plan scheduled for July

1.5. *Top 10 Risks*

Top 10 risks are attached. No change from last month.

IMPACT Top Ten Risks 4/2002

No.	Risk Item	Score	Mitigation	Mitigation Schedule						
				PDR	Bread-board Test	CDR	Sub-system Test	System Test	Env test	Early Orbit Test
UCB_5	IMPACT boom is a new design. Failure could affect Imager pointing requirements as well as boom-mounted instruments.	HIGH	Design for reliability. Early development and test to ensure reliability.	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH
UCB_21	Custom VLSI used in SEP may has schedule and cost risk	MEDIUM	Early development to prove design; use Amptek in place of VLSI in SIT (still use VLSI in HET, LET)	MEDIUM	MEDIUM	LOW	LOW	LOW	LOW	LOW
UCB_23	Non-standard parts qualification failure could impact delivery schedule	MEDIUM	Early parts selection and screening	MEDIUM	MEDIUM	LOW	LOW	LOW	LOW	LOW
UCB_15	GSFC Approval Requirements could delay instrument delivery or add cost	MEDIUM	Difficult to asses, history is mixed	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	LOW
UCB_4	The IDPU is a single point failure mechanisim for the IMPACT suite and PLASTIC	HIGH	IDPU is a simple, reliable system. Extra attention will be paid to ensuring its reliability	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH
UCB_13	IMPACT team is thin; loss of a critical team member could delay delivery	MEDIUM	Reassign work amongst team as and when required	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	LOW	LOW
UCB_11	Stringent EMI requirements may delay schedule if testing fails	MEDIUM	Careful design, early testing	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	LOW	LOW
UCB_1	ITAR restriction of information exchange with foreign CoIs may result in problems not discovered until late in the program	MEDIUM	Various channels of communication have been found within the ITAR restrictions to allow adequate information flow. Some exchanges are still forbidden and may cause a problem.	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	LOW
UCB_18	LET Detectors from a new manufacturer	MEDIUM	Backup L1 dtectors ordered; low risk, meet requirements	MEDIUM	MEDIUM	LOW	LOW	LOW	LOW	LOW
UCB_10	Complex Interlocking IMPACT schedule increases risk of late delivery to spacecraft	MEDIUM	A milestone schedule of deliveries has been set up to minimize schedule interaction and give power to control schedule to institutions while maintaining top level schedule slack; an integrated Project-level schedule is in progress. It is not clear yet if this will actually reduce risk	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	LOW	LOW

2. Berkeley Status

2.1. *Summary of Status*

The UCB schedule with updated status will be delivered separately.

2.2. *Major Accomplishments*

SWEA/STE:

- LBNL completed noise reduction work on STE CSA. In test at UCB.
- SWEA/STE layout work in progress.
- SWEA/STE FPGA design in progress.
- Completed analysis of STE calibration radiation source requirements; starting to work with manufacturers on how to make it.

IDPU:

- Data Controller Board ETU complete and in FPGA testing.
- Flight Software: Add EEPROM & housekeeping code.
- CRÈME analysis of flight SRAM SEU sensitivity indicates significant error rate during solar flares (for a 16kbyte code we would get a bit error every few days during a large flare). This is acceptable for data and tables (with some error checking added), but not for code (we don't want to crash just when the data gets interesting). Changed baseline to run from EEPROM instead of RAM.

LVPS/HVPS:

- IDPU LVPS ready for layout, waiting on availability of layout person.
- SIT HVPS in layout

Boom:

- Thermal model proceeding (with Eby).
- Boom FEM delivered to APL, working conversion issues
- Prototype / Flight tube bids are in, place order shortly.
- Working on details of rings

GSE:

- IDPU Simulator complete. Instrument-specific work in progress (MAG, SWEA/STE).
- Work for C&T GSE in progress (Command encoder, MOC Interface); telemetry displays pending telemetry specification.

2.3. *Design Updates*

STE-U location may move (in discussion with APL)
STE radiation source

2.4. *Outstanding Problems*

- Operational heater power budget over allocation
- Problem with space at the sunny end of the boom; can be mitigated by moving STE-U.

2.5. *New Problems*

None.

2.6. *Top Risks.*

No new risks identified.

2.7. *Problem/Failure Quick Look*

None.

3. GSFC (SEP) Status

STEREO/IMPACT/SEP/GSFC Progress Report for MAY, 2002 – (von Rosenvinge, Baker, Hawk, Reames, Shuman, Wortman)

3.1. *Summary of Status*

Mostly on-schedule. The HET H1 detector mount has been sent out for fabrication and quotes have been requested for the H3 mount. The PCB layout for the LET2 and LET3 detector mounts is about to begin. A list for procuring all detector connectors has been completed. The PCB coupons for the L1 detector mounts have been submitted for GSFC analysis.

Micron had notified us last month that acrylic polymers are inconsistent with chemicals used by them for detector cleaning. The LET L1 detector mounts are the only ones manufactured so far, but they were assembled using an acrylic bonding material. We have now resolved this issue with Micron and the acrylic polymer will be satisfactory (Micron will modify their cleaning procedure somewhat). This freed us up to go ahead with the H1 mount procurement.

3.2. *Major Accomplishments*

Bob Baker has made additions to the MISC design to make our design compatible with recent additions that Caltech has made to their design. Specifically, the g-bus commands have been extended for communication with the Caltech ASIC and the MISC now generates a one-minute interrupt when the 1-sec signal from SEP Central is double-pulsed.

Work has been continuing to develop the GSE and MISC software that we will need shortly to test the Caltech PHA ASIC. Caltech is sending us this week a test board with an ASIC chip mounted to it for test. The chip is mo unted directly to a PC board so that we can start learning how the chip works as well as look for any possible residual design problems. This approach will help save considerable time since we don't have to wait until the new chip hybrid package is completed.

George Winkert has begun work on the front-end logic for SIT. He will have produced a pin-out by the first week in July, consistent with Peter Walpole's schedule for laying out the board on which the MISC/front-end Actel chip will be mounted.

3.2.1. Next month-

- Complete the L2 and L3 detector mount designs.
- Continue work on the HET GSE, on-board software, and PHA ASIC test software.
- Start testing the PHA ASIC.
- Continue development of the preliminary front-end electronics design for SIT.
- Deliver a thermal model to APL.

3.3. *Design Updates*

None quantified this month.

3.4. *Outstanding Problems*

No major problems outstanding.

3.5. *New Problems*

None.

3.6. *Top Risks*

No significant risks at GSFC? Need to ensure that manpower becomes available per the current plan. Work on the SIT front-end electronics design was delayed due to availability of the engineer responsible for this. He has now started work on this task and he can meet the schedule. He has already reviewed the requirements and sees nothing that is not straightforward.

3.7. *Problem/Failure Quick Look*

4. Kiel (SEPT) Status

SEPT Monthly Technical Progress Report
May 2002

4.1. *Summary of Status*

1. Updated SEPT outline drawing distributed, cardboard model sent to John Hawk.
2. Canberra detectors received 2nd layer of vacuum deposited aluminium for light tightness.
3. Monte Carlo simulation results show efficient magnetic deflection even for high energy electrons, but higher threshold for low energy protons. Go-ahead issued for assembly of flight magnet systems.
4. Digital board fully assembled and tested.
5. Analog board over 90 % assembled, housekeeping read out needs still bread-boarding. PDFEs fully assembled. PDFE test reveals noise problems, currently under investigation.
6. EGSE ready and working, waiting for feedback for further improvement and increased functionality.
7. ESTEC PA plan submitted, negotiations with Dave Curtis and STEREO project continue.

4.2. *Major Accomplishments*

1. A mock-up of SEPT to serve as a model for thermal issues like MLI tailoring is sent to John Hawk, together with an update of the mechanical interface control drawing. The changes are described in last months progress report.
2. In an effort to improve light tightness, a second layer of aluminium was deposited on the Canberra detectors following a recommendation by Tycho to avoid pinholes. The total dead layer of the detectors now amounts to 120 nm Al (1st step) + 50 nm Al (2nd step) + 150 nm n+ silicon implantation layer.
3. The mathematical model was improved by implementing a more realistic magnetic field model that tapers off at the edges of the magnets and is not zero outside. This field configuration was verified by point measurements using the prototype magnet system. First results show: even 1 MeV electrons are efficiently deflected (goal was 400 keV), while 55 keV protons are deflected by 8°, shifting slightly the cone of incidence. Based on this outcome, the manufacturer of the magnet system was given the go-ahead for assembly of the 4 flight systems and 1 spare system.
4. The mathematical model was improved by adding different detector dead layers with the thickness as parameter. The result of the dead layer study showed a lower threshold for protons of 55 to 60 keV as opposed to 30 keV given in our level 1 science requirements. This threshold increase is a trade-off of our efforts to reduce stray light sensitivity by mounting the detectors with their Ohmic side out. We looked into ways to mitigate this consequence, e.g. by mounting those detectors with unobstructed field of view with their junction side out. However, the existing high voltage and grounding design as well as the possibility of stray light even from surfaces not in the direct field of view are prohibitive. A proton accelerator run is needed to verify the mathematical model in the range 30 keV to 2 MeV.

5. Digital Board
   - Fully assembled, tested and working (DAC, SRAM, FPGA, interface)
   - Interface PC to SEPT working
   - SEPT commander ready (test software for emulating SEP DPU and testing of SEPT-SEP -communication)
   - Simulator (Visual Basic application) of FPGA is ready
   - DB-calibration circuit working (test pulses with wrong pulse polarity, some oscillations)
6. Analog Board
   - Four PDFE's are mounted, boards fully assembled
   - Testing in progress – almost complete
   - Update of schematic done (includes bias current read out)
   - Noise is still too large, could be strongly reduced (ringing source found). Source not completely understood – replacement of 2.5V reference proposed. (20 µVpp to 1.5 µVpp)
   - Box provided
   - New solution for connectors: tri-axial replaced by coaxial (Suhner) internal
   - Bias current read out needs to be bread-boarded
7. Test board for Analog Board
   - Of minor priority now – required later for EM and FM
   - Fully assembled, few bugs
   - Some signals with wrong direction (needs investigation)
   - Need to make new PCB with board cutout to allow access to lower side of the Analog Board
   - Has a few lines missing (2 serial lines) – can be repaired by hand wiring and use of spare pins
   - Software for the AB-Test Board finished
8. EGSE computer
   - Fully working
   - EGSE allows tuning every parameter of the FPGA and analog part and display data in real time = growing product (parts are included when needed)
   - Needs now feedback by test personal for further improvement
   - Automatic detection of FPGA version
9. ESTEC man power
   - New Technical Manager: Ludovic Duvet, succeeds Peter Falkner starting 1-JUL-02
10. PA/QA
    - ESTEC PA Plan submitted, currently under negotiation
    - Component testing in progress (radiation test with Co-60, latch-up test with proton test facility, thermal stressing (all parts in extended temperature range –40°C to +85°C)
    - Parts list updated, replaceable parts identified

4.3. *Design Updates*

- A waiver should be sought to change the level 1 science requirements to reflect the 55 keV threshold for ions (see above Major Accomplishments item 4).

4.4. *Outstanding Problems*

Inconsistency of Kiel schedule and ESTEC schedule will be resolved after completing the first integration of detector system and associated electronics, now scheduled for July/August 2002.

4.5. *New Problems*

Noise measurement of analogue electronics shows unacceptable high values. Investigation ongoing. New test at ESTEC in week of 9-JUN-02 (without detectors). New test with detectors scheduled for July/August 2002 (vacation time problem).

4.6. *Top Risks*

4.7. *Problem/Failure Quick Look*

5. Caltech/JPL (SEP) Status

May 2002

5.1. *Summary of Status*

Activities centered on detector development, electronics development, and flight and GSE software development.

Major Accomplishments

Reviews:

- A software and schedule review was held on 21-22 May 2002 at Caltech.

Detectors:

- Two additional silicon wafers with front-side patterning done by Micron Semiconductor were received by JPL for thinning. The thinning was delayed because of a change of personnel available at JPL to apply the gold masking needed prior to thinning. A technician has been identified who can handle this task and he is now nearly up to speed on the processing we need done.
- Micron received the 20-micron-thick, 3-inch diameter wafers that they had ordered from Virginia Semiconductor. These will be used for producing L1 prototypes without thinning ("plan B"). The processing has started on an initial set of 4 of these wafers. The masks needed for doing the photolithography on these devices have also been ordered.
- Micron's work on the prototype L2, L3, H1, and H3 detectors is on hold waiting for receipt of detector mounts. The mount design and fabrication work is progressing at GSFC. Micron reports that based on their wafer-level testing they expect that all of the prototype detectors (other than L1) can be obtained from the wafers that have already been processed

Electronics:

- A single VLSI chip was wire-bonded to a test PCB and has been studied fairly extensively. A copy of the test set is nearly ready to be sent to GSFC.
- With the exception of problems listed below the chip functions properly. PHA transfer functions exhibit good temporal stability and linearity (integral non-linearity of less than 0.02% of full scale). Differential non-linearity (variation of channel widths) is less than 5%. In general, the analog and digital sections operate properly, without substantial interference from the digital to analog sections.
- Problems with VLSI:
    1. Glitch at time of linear gate reopening produces extra deadtime (10-30 usec per event). This is serious enough to require a re-spin. The problem is now well understood and there is a low risk design mod.
    2. Powered down PHA channels introduce a small spurious current onto the diagnostic readout buss, producing about a 20 mV dc shift of observed signals per powered-down channel. This problem does not affect normal operation, but will be fixed in the re-spin.
    3. Cross-talk exists between different PHA channels on a given VLSI chip. The nature and significance of the cross-talk are still being explored. The cross-talk

is approximately at anticipated levels and results from the sharing of power and ground busses across all 16 PHAs on a given VLSI chip. Any minor modification in the power bussing on-chip that might improve the cross-talk situation will be considered for the re-spin.

- Re-spin wafer fab is anticipated to begin in August or September of 2002. (This is contingent on the outcome of total dose and latchup radiation testing scheduled for July.)
- AMI foundry quoted the same price for VLSI re-spin as for the original run ($77,500). The plan is to share this run with another chip design in our lab, so the cost to STEREO should be $38,750.
- The current chips are adequate to proceed with a first hybrid build of a few parts.
- Held Hybrid PDR at JPL.
- Ordered flight EEPROM from Maxwell Technologies (formerly Space Electronics).
- Continued work on flight parts selection.
- Bias supplies (report from Dean Aalami, Space Instruments):
    1. The bias supply consists of a basic power supply with +300 V and –200 V outputs and a +100 V tap from the multiplier stack. There are 5 post regulators which provide the desired detector outputs and current limiting. The function of the high voltage post regulators is to provide well regulated outputs with sharp current limiting.
    2. Preliminary designs of the basic supply and the HV post regulators are complete. The designs have been verified by SPICE analysis. A 4-layer PCB has been procured and parts are being gathered to fab the proof of concept board. This board will be the same size as the final configuration.
    3. A preliminary parts list has been submitted.
    4. Remaining work:
        - Procure or obtain parts for the proof of concept board.
        - Fab proof of concept board.
        - Test proof of concept board.
        - Finalize schematic and parts list.
        - Layout boards.
        - Support fab & test.
- Analog/Post-regulator board (report from Dean Aalami, Space Instruments):
    1. Preliminary design of the Analog/Post-reg board is complete. A preliminary layout study using the near final design has been performed and the preliminary design fits the allocated board size.
    2. The Analog/Post-reg board houses three +5 V regulators to proved the +5A outputs. It also includes Analog housekeeping multiplexers and an A/D converter.
    3. A preliminary parts list has been submitted.
    4. Remaining work:
        - Finalize schematic and parts list.
        - Layout board
        - Support fab & test.
- Resource update: no changes, except that packet headers are now included in the SEP telemetry allocation

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Software:

- Prepared LET/SEP-Central Software Requirements document.
- Prepared for software requirements review May 21.
- Worked on build 1 of LET onboard processing software.

GSE:

- Detector Development System - No work.
- Began work on the Graphical User Interface (GUI) code for handling the page display windows for LET. This is Java code that creates and manages the windows which will contain the LET page displays and responses to the user's mouse and keyboard inputs. This code is independent of the data format. The code that filters the packets, extracts data structures, and builds the page display models which form the contents of the windows is not part of this activity. That code is dependent on the data format and cannot be designed until the data format is finalized.

5.2. *Design Updates*

- No changes to mass and power estimates. Bitrate allocation now includes packet headers.

5.3. *Outstanding Problems*

None.

5.4. *New Problems*

- Cost for re-spin is not in Caltech budget.

5.5. *Top Risks*

- The budget is very tight with no reserve being held at Caltech.
- Schedule slack that we show explicitly will be taken away from us.
- Development of the L1 detector. (See April and September reports for details.) Risk mitigated by creating slack in schedule and by starting a parallel development effort using different and more conventional manufacturing technique.
- Development of the VLSI chip. (See September report for details.) Risk mitigated by providing for two more months for the layout and checking while still keeping 30 weeks for a second run if necessary. Also, initial chip fabrication happened much faster than anticipated which is helpful if another run is needed.

5.6. *Problem/Failure Quick Look*

None.

6. SIT MONTHLY TECHNICAL PROGRESS REPORT
May 2002

6.1. *SUMMARY of STATUS*

a. SIT TELESCOPE - Prototype is in house and working.

b. SIT TOF System - Flight boards have been fabbed and coupon testing is underway.

c. SIT Energy/Logic System - Prototype energy system under test with GSE logic board

d. SIT HVPS - HVPS ETU fabrication in process

6.1.1. Schedule Changes

The schedule is currently under review. We are working with scheduler Robert Palfy to bring our schedule in line with the rest of the SEP schedule. An updated schedule will be submitted when this is complete.

6.2. *MAJOR ACCOMPLISHMENTS*

6.2.1. This Month

Energy - Some progress was made on the energy system but it is taking longer than anticipated.

TOF - The TOF system was checked with the new Actel chip. Calibration and characterization of the system was performed

Software - We defined and submitted to GSFC the algorithm for classifying pulse height events into matrix rates. We also began defining the details of the remaining SIT flight software requirements.

6.2.2. Next Month

We will finish testing the energy system on its own and integrate it with the prototype TOF system.

6.3. ***DESIGN UPDATES***

6.3.1. Resources

	Last Month	This Month	Change
Mass (g) *	1336	1336	0
Power (mW)	1354	1354	0
Telemetry (bps)	418	418	0

* Includes 200g bookkept by GSFC for SIT structure

6.4. ***OUTSTANDING PROBLEMS***

6.5. ***NEW PROBLEMS***

6.6. ***NEW RISKS***

6.7. ***PROBLEM/FAILURE QUICK LOOK***

Starts at first turn-on of flight hardware.

ID #	Description	Assignee	Opened	Closed

7. CESR (SWEA) Status

CESR- TOULOUSE- FRANCE **Author : Claude Aoustin / Project Manager**

SWEA PROGRESS REPORT # 9
(June 14, 2002)

May 2002

CESR is in charge of :
- Electrostatic analyzer with deflectors, grids and Retractable Cover
- Detector consisting of two MCP rings
- Amplifiers and discriminators
- 3 High voltages

7.1. *Summary of Status*

Mechanical design end 17/12/2001 completed
Mechanical analyzer fabrication end 22/04/2002
Quite finished for the ETU (99 % done)
Electronics fabrication completed under test (50% tested).
ETU Assembly start 17/06/2002 end 07/2002
Delivery to UCB was planned for 12/07/2002 : will be delayed !

7.2. *Major accomplishments*

Mechanical fabrication:
- First EM analyzer and housing fabricated.
- Deflector grids fabrication: one set (2 grids) fabricated. Transparency lower than expected (75% per grid). Could be increased for the flight models if necessary by having bigger cells.
- Spheres treatment and black coating finished. Spheres received in Toulouse.
- Integration will start in June. Delayed due to the difficulty to get the grids within the expected time.
- Verification under vacuum in July.

Electronics boards are designed, fabricated, populated and under test.

Pin Puller arrived in Toulouse. Given to the subcontractor. Mechanical support under fabrication.

7.3. *Design Updates*

Mass : 1040 g
Power : 446 mW min ; 662 mW max

7.4. *Outstanding Problems*

AMPTEKS amplifiers quality:
- additional burn in will be done : 1000h at 125°C on 10 pieces.
- specification given to Hirex : subcontractor specialized for testing flight parts.

7.5. *New problems*

None

7.6. *Top Risks*

7.7. *Problem Failure Quick Look*

None

8. GSFC (MAG) Status

Nothing to report.

9. EPO at UCB

Nothing to report