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Subject: IMPACT Monthly Technical Progress Report, Contract NAS5-00133

Harry:

Enclosed is the monthly technical progress report for the STEREO IMPACT project for the month of April 2002.

Sincerely,

David Curtis
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CC:

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IMPACT Team

1. IMPACT Overview

This report is presented in sections by institution. Section 1 is an IMPACT Project Manager / System Engineer's overview.

1.1. *Contracting / Funding*

A new funding allotment to cover through June has been received by UCB. Corresponding allotments to subcontractors are in work. Because of pipe-line delays in the system through to the subcontractors (Caltech and UMd) it is important that IMPACT be funded somewhat in advance of expected spending.

We have submitted a revised budget for the launch slip after a few iterations and some decreases in level of effort.

1.2. *Significant System-Level Accomplishments*

- Working EMC issues; submitted waivers for single-ended interfaces, STE door actuator.
- Updated the IMPACT Performance Requirements to flow down from the Level 1 requirements in the MRD.
- IMPACT Configuration Management Plan: Project submitted a proposed modified (expanded) version; we have returned comments.
- PAIP: Working the ESTEC appendix (the last hurdle). Project comments to the latest version have been forwarded to ESTEC.
- Updated the IMPACT Grounding diagram
- Participated in Ground Systems PDR at APL
- Submitted proposed dates for pre-CDR Peer Reviews
- Worked with Project planner on integrated schedule
- Still working on parts screening issues (selecting contractors, developing details test specs), getting approvals

1.3. *System Design Updates*

Change in location of STE-U under consideration to alleviate space issues at sunny end of boom (working with APL).

1.4. *System Outstanding Issues*

- ESD issues with sun-facing surfaces (ITO contamination issue vs Goddard Composite Coating). We need to better understand the GSFC Composite Coating properties)
- Need to arrange a team Data Analysis meeting to outline Data Analysis Plan.
- Need to submit a STE calibration source plan to Project & Instrument teams (pending determination of required source strength)

1.5. *Top 10 Risks*

Top 10 risks are attached. A resolution to UCB_21 is expected soon; the first parts have been delivered and are in test.

IMPACT Top Ten Risks 4/2002

No.	Risk Item	Score	Mitigation	Mitigation Schedule						
				PDR	Bread-board Test	CDR	Sub-system Test	System Test	Env test	Early Orbit Test
UCB_5	IMPACT boom is a new design. Failure could affect Imager pointing requirements as well as boom-mounted instruments.	HIGH	Design for reliability. Early development and test to ensure reliability.	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH
UCB_21	Custom VLSI used in SEP may has schedule and cost risk	MEDIUM	Early development to prove design; use Amptek in place of VLSI in SIT (still use VLSI in HET, LET)	MEDIUM	MEDIUM	LOW	LOW	LOW	LOW	LOW
UCB_23	Non-standard parts qualification failure could impact delivery schedule	MEDIUM	Early parts selection and screening	MEDIUM	MEDIUM	LOW	LOW	LOW	LOW	LOW
UCB_15	GSFC Approval Requirements could delay instrument delivery or add cost	MEDIUM	Difficult to asses, history is mixed	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	LOW
UCB_4	The IDPU is a single point failure mechanisim for the IMPACT suite and PLASTIC	HIGH	IDPU is a simple, reliable system. Extra attention will be paid to ensuring its reliability	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH
UCB_13	IMPACT team is thin; loss of a critical team member could delay delivery	MEDIUM	Reassign work amongst team as and when required	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	LOW	LOW
UCB_11	Stringent EMI requirements may delay schedule if testing fails	MEDIUM	Careful design, early testing	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	LOW	LOW
UCB_1	ITAR restriction of information exchange with foreign CoIs may result in problems not discovered until late in the program	MEDIUM	Various channels of communication have been found within the ITAR restrictions to allow adequate information flow. Some exchanges are still forbidden and may cause a problem.	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	LOW
UCB_18	LET Detectors from a new manufacturer	MEDIUM	Backup L1 dtectors ordered; low risk, meet requirements	MEDIUM	MEDIUM	LOW	LOW	LOW	LOW	LOW
UCB_10	Complex Interlocking IMPACT schedule increases risk of late delivery to spacecraft	MEDIUM	A milestone schedule of deliveries has been set up to minimize schedule interaction and give power to control schedule to institutions while maintaining top level schedule slack; an integrated Project-level schedule is in progress. It is not clear yet if this will actually reduce risk	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	LOW	LOW

2. Berkeley Status

2.1. *Summary of Status*

The UCB schedule with updated status will be delivered separately.

2.2. *Major Accomplishments*

SWEA/STE:

- Efforts to reduce STE noise level proceeding at LBNL
- SWEA/STE layout work started.
- SWEA/STE mechanical design complete.
- SWEA/STE FPGA design in progress.

IDPU:

- Data Controller Board 2nd layout complete and in fab (first layout had a problem).
- Data Controller Board FPGA complete, ready to test when ETU DCB complete.
- Flight Software: Command Routing, System Command decoding, Watchdog complete.

LVPS/HVPS:

- IDPU LVPS nearly ready for layout.
- SIT HVPS nearly ready for layout (pending resolution of mechanical issues)

Boom:

- Thermal model proceeding (with Eby).
- Review of boom status/design with Project
- Prototype / Flight tube specifications complete, out to bid.

GSE:

- IDPU Simulator complete. Instrument-specific work in progress (MAG, SWEA/STE).
- Work for C&T GSE in progress (Command encoder, MOC Interface); telemetry displays pending telemetry specification.

2.3. *Design Updates*

STE-U location may move (in discussion with APL)

2.4. *Outstanding Problems*

- Operational heater power budget over allocation
- Problem with space at the sunny end of the boom; can be mitigated by moving STE-U.

2.5. *New Problems*

None.

2.6. *Top Risks.*

No new risks identified.

2.7. *Problem/Failure Quick Look*

None.

3. GSFC (SEP) Status

STEREO/IMPACT/SEP/GSFC Progress Report for March, 2002 – (von Rosenvinge, Baker, Hawk, Reames, Shuman, Wortman)

3.1. *Summary of Status*

Mostly on-schedule. The HET H1 and H3 detector mount designs are now complete and the LET L2 and L3 mount designs have been started. The H1 and H3 mount designs were reviewed by the detector manufacturer (Micron) and design changes were incorporated as a result. Specifically, concerns about the relative thermal expansion of Si and epoxy fiber glass have caused us to revise the way that we electrically connect the backsides of the detector wafers to the flex-circuit.

Micron has just notified us that acrylic polymers are inconsistent with chemicals used by them for detector cleaning. The LET L1 detector mounts are the only ones manufactured so far, but they were assembled using an acrylic bonding material. Consequently we may have to remanufacture the L1 mounts. So far Micron is not ready to use the L1 mounts, but they are ready for the H1 and H3 mounts, so we are trying to resolve the issue of acrylic bonding material and get the H1 and H3 mounts manufactured as soon as possible.

Finishing the L2 and L3 mount designs depends upon final location of the connectors on the LET analog board. The new ASIC hybrid package is larger than what had previously been planned and we had made a scaling error in our initial conceptual layout, so the LET layout is much tighter than originally anticipated. As a result, PHA ASICs will be placed on both sides of the LET analog board and the number is being reduced from six to four.

3.2. *Major Accomplishments*

Tycho von Rosenvinge, Larry Ryan, and Sandy Shuman spent one full day at Caltech in early April reviewing the LET design with Rick Cook and Branislav Kecman. This visit was very useful since it helped to flush out the LET layout problems alluded to earlier.

Work has been underway to develop the GSE and MISC software that we will need shortly to test the Caltech PHA ASIC. Caltech will be sending us very soon a test board with an ASIC chip mounted to it for test. The chip is mounted directly to a PC board so that we can start learning how the chip works as well as look for any possible residual design problems. This approach will help save considerable time since we don't have to wait until the new chip hybrid package is completed.

3.2.1. Next month-

Complete the L2 and L3 detector mount designs.
Continue work on the HET GSE, on-board software, and PHA ASIC test software.
Expand the GSFC MISC design to accommodate extensions to the Gbus.
Start testing the PHA ASIC.
Develop preliminary front-end electronics design for SIT.

Review the thermal design.

3.3. *Design Updates*

None quantified this month. The LET total weight may increase somewhat with the double-sided analog board.

3.4. *Outstanding Problems*

No major problems outstanding.

3.5. *New Problems*

None.

3.6. *Top Risks*

No significant risks at GSFC? Need to ensure that manpower becomes available per the current plan. Work on the SIT front-end electronics design has been delayed due to availability of the engineer responsible for this. He will be starting work on this task by the third week in May and the schedule can tolerate this. He has already reviewed the requirements and sees nothing that is not straightforward.

3.7. *Problem/Failure Quick Look*

4. Kiel (SEPT) Status

SEPT Monthly Technical Progress Report
April 2002

4.1. *Summary of Status*

- SEPT outline drawing revised.
- SEPT grounding scheme revisited.
- Mathematical model of SEPT sensor generated.
- Prototype magnet system tested at GSFC.
- SEPT cardboard model built to serve as a mock-up for John Hawk and MLI tailor.

4.2. *Major Accomplishments*

- The revised SEPT outline drawing includes now two thermostats 4BT-2 and shows the 9-pin actuator connector in the same position but rotated by 90°.
- The SEPT grounding scheme was revisited with the goal of avoiding triax cables and connectors, which are deemed too bulky and too heavy by Dave Curtis. Current plans look promising, making announcement of weight increase in last month's progress report obsolete.
- A mathematical model of the SEPT sensor was generated using GEANT (from CERN library) with zero order approximation of the magnetic field in the air gap (square wave profile: 5000 Gauss between magnets, 0 Gauss outside). Result: 1 MeV electrons are efficiently deflected, but some non-negligible percentage of 20 keV protons are deflected as well, which was not the intention. More realistic field configuration is being incorporated into the mathematical model. This field configuration was calculated by the manufacturer and verified by measurements at a few positions.
- The prototype magnet system was tested at GSFC. Mario Acuna is satisfied with the test results: 1.4 nT far field calculated at 3 m distance with ideal (= perfectly matched) magnets, 1.6 nT far field calculated with mismatched but carefully selected magnets, 1.8 nT measured by Mario Acuna. The measured far field falls off as r^{-3}, i.e. it is a dipole as expected. No need for mu-metal shielding or compensation magnets.
- Discussions with John Hawk led to some clarifications w.r.t. the thermal design. It became clear that a SEPT mock-up would be needed to serve as a model for tailoring the MLI. This model was built but not yet shipped to John Hawk.
- Testing of the analogue and digital electronics at the Swedish subcontractor site continued. Noise problems in the analogue ASIC (PDFE) were observed making further studies necessary. This delays the first system test with detectors originally planned for mid May.

4.3. *Design Updates*

Actuator connector (9-pin D subminiature) rotated by 90°. Note: the most recent design change for triax cables RG-403 and NDL-T connectors (see last month's progress report) may be reversed back to coax cables RG-178 and SSMC connectors pending a final decision in the next weeks.

4.4. *Outstanding Problems*

Inconsistency of Kiel schedule and ESTEC schedule will be resolved after completing the first integration of detector system and associated electronics, now scheduled for June 2002.

4.5. *New Problems*

4.6. *Top Risks*

4.7. *Problem/Failure Quick Look*

5. Caltech/JPL (SEP) Status

April 2002

5.1. *Summary of Status*

Activities centered on detector development, electronics development, and flight and GSE development. The rapid response by the AMI foundry on the fabrication of the VLSI wafers bodes well if another run is required. Good progress is being made with the detectors, although the L1 detector continues to provide the biggest challenge.

5.2. *Major Accomplishments*

Detectors:

- A meeting was held at Caltech on April 22 with representatives from Micron Semiconductor, Caltech, and JPL, and a telephone tie-in to GSFC to review status of the LET/HET detector development.
- Etching of a second silicon wafer that had front-side patterning for the LET L1 design was attempted. The cracking of the wafer that occurred on the first attempt did not reoccur. However, a new problem was encountered—after etching about half-way through the 300 micron thick wafer, the etch rate accelerated significantly over portions of the area being thinned that were correlated with the implanted pattern on the opposite side of the wafer. The implanted ions that form the pattern have a range of only about 0.5 microns and yet this pattern was apparently being "sensed" from a distance of nearly 150 microns. After researching this problem in the literature and not finding reports of previous occurrences of this sort, additional etching tests were done with test pieces taken from the first wafer that was partially etched in March. The accelerated etching problem was not reproduced. It was agreed that etching of another full wafer with front side patterning should be tried. Micron shipped two additional patterned L1 wafers for further etching tests.
- Micron has ordered the lapped and polished 3-inch diameter, 20 micron thick wafers needed for the backup L1 development plan from Virginia Semiconductor. This vendor cannot guarantee the thickness uniformity required for the L1 detectors, so we will need to measure at least a sample of the wafers when they are delivered to see whether or not they meet our uniformity requirements.
- Micron has completed all of the wafer-level processing of the thicker LET/HET detector designs (L2: 50 microns; L3, H1, and H3, all 1000 microns). The quantities are as follows:

L2	3 wafers with 1 L2 detector on each wafer
L3 & H1	4 wafers with 2 H1 detectors and 1 L3 detector on each wafer
H3	2 wafers with 2 H3 detectors on each wafer

  All of these devices look good based on wafer-level testing. Micron is now waiting to receive detector mounts from the HET/LET team in order to dice the wafers, mount the detectors, and do detailed testing.
- Micron Semiconductor reviewed the designs for the H1 and H3 detector mounting and recommended against making direct electrical contact between the silicon wafer and traces on the G10 mount using rigid conductive epoxy because of concerns over possible problems with differential thermal expansion between the silicon and the G10. It was decided to follow Micron's advice and make the back side contacts using fine silver wires attached with conductive epoxy, since the wire is flexible enough to

take up the differential motion. Front-side contacts on H1 and H3 will be made by ultrasonic wire bonding, as previously planned.

- The L1 detector mount design (done by GSFC) is essentially ready for fabrication. The only outstanding question is whether it will be necessary to eliminate a redundant row of connector pins in order to conserve space on the board that holds the front-end electronics.

Electronics:

- We received two 8" VLSI wafers from the AMI's foundry well ahead of schedule. The wafers were then thinned and diced by Corwil Technology Corp., yielding a total of 840 die.
- In lieu of hybrid packaging, a test PCB for quick VLSI functional check was designed and fabricated. The test set consists of the small PCB coupled to an existing MISC development board. Two PCBs were assembled with VLSI die and some of hybrid components were wire-bonded directly to the PCB. One test fixture box was fabricated, and the second one will be finished and shipped to GSFC soon.
- Initial tests have been done with the test set and one die.
- After only two days of testing the chip seems to function as it should, but not all functions have been exercised on the relatively complex chip. The on-chip command register can be loaded and each of the 16 on-chip PHAs separately powered. Power consumption is as expected. The on-chip diagnostic system is working, allowing the routing of test points to two on-chip precision unity gain buffer amps that drive off-chip to provide for oscilloscope viewing. The on-chip built-in test pulsers of each preamp input function properly. Test signals of the proper shape have been observed at various test points including preamp, postamp and amplifier-offset-gate outputs; however full pulse-height analysis and readout of digital data have not yet been attempted.
- Testing continues with high priority to identify any problems that might require a "re-spin".
- Schematics and part selection for the ASIC hybrid were finalized. Layout of the hybrid's ceramic substrate was started at JPL and a metal package was selected which will fit all components with conservative layout guidelines. All hybrid parts are on order except for the substrate and lid.
- A preliminary layout of the LET front-end board has been done using the new PHA hybrid package. Position of connectors from the L1, L2 and L3 detectors was adjusted to allow plenty of room for the routing of their signals, etc.
- The work indicates that we have room for only 4 (not 6) PHA hybrids. We therefore decided to drop the 6-unit option.
- We had a productive visit with GSFC team members on wide variety of topics and electro-mechanical issues related to HET/LET/SEP Central Electronics.
- After a long search we located a forced-air temperature controller unit at JPL which will be available for flight hybrid screening at Caltech. Hybrid test fixture with ZIF socket will be designed to fit the controller's nozzle for cooling and heating of the hybrid package.
- Attached resource summary table includes minor mass increase in HET and LET due to the metal hybrid package and associated hardware. No updates from SIT and SEPT for this month.

Software:

- Worked on completing requirements and design prior to starting on the first build of LET onboard data processing software.

GSE:

- Detector development system - No activity
- GSE - tried to clarify the commanding requirements on the SEP During April, the issue of commanding requirements on the SEP GSE arose thru a series of e-mails concerning remote commanding. Even though the commanding requirements that the SEP GSE software must implement have not been formally defined, remote commanding was not a mode that was anticipated. Conceptually, from the GSE software point of view, remote commanding means that there will be two sources of commands instead of one. At Caltech, there should not be any major difficulty in providing software that manages commanding from more than one source. After delivery to UCB, the SEP GSE software could be written in such a manner that commands could be forwarded to the IMPACT GSE thru a TCP/IP socket (as long as UCB is willing to furnish the socket). However, most of the issues involved in remote commanding are not GSE software issues (even though there are some software impacts). Some of the issues which would have to be addressed are availability, network security, and command authentication. In addition, the people responsible for operating the instruments will need to accommodate remote commanding in their procedures. The plan is to let non-GSE issues decide whether a remote command ability should be part of the GSE software. At that time the appropriate interfaces and software can be defined.

5.3. *Design Updates*

- No changes to mass and power estimates.

5.4. *Outstanding Problems*

None.

5.5. *New Problems*

- See description of new problem in etching wafers to make L1.

5.6. *Top Risks.*

- The budget is very tight with no reserve being held at Caltech.
- Schedule slack that we show explicitly will be taken away from us.
- Development of the L1 detector. (See this report and September report for details.) Risk mitigated by creating slack in schedule and by starting a parallel development effort using different and more conventional manufacturing technique.
- Development of the VLSI chip. (See September report for details.) Risk mitigated by providing for two more months for the layout and checking while still keeping 30 weeks for a second run if necessary. Also, initial chip fabrication happened much faster than anticipated which is helpful if another run is needed.

5.7. *Problem/Failure Quick Look*

None.

6. SIT MONTHLY TECHNICAL PROGRESS REPORT

April 2002

6.1. *SUMMARY of STATUS*

a. SIT TELESCOPE - Prototype is in house and working.
b. SIT TOF System - Flight modifications to Prototype electronics design and layout are underway.
c. SIT Energy/Logic System - Energy system redesigned with Amptek parts. Preliminary design and prototype layout completed. PC Board received, assembled and under test.
d. SIT HVPS - HVPS ETU fabrication in process

6.1.1. Schedule Changes

None. The energy system testing is taking longer than planned and we are a couple of weeks behind the schedule issued 1/22/02 and updated with latest progress 5/9/02. No impact on the remainder of the schedule is anticipated.

6.2. *MAJOR ACCOMPLISHMENTS*

6.2.1. This Month

Energy - The prototype energy board was assembled. The readout logic was implemented in Xilinx and tested. A test program was written in LabView and testing of the energy system has begun. Gains and pulse shapes have been trimmed and the system works to first order. There are still some bugs and it is taking somewhat longer than anticipated to get everything working together. We are a couple of weeks behind where we expected to be at this point.

An update of the front-end logic requirements document including the new energy design was generated and submitted to GSFC.

6.2.2. Next Month

We will finish testing the energy system on its own and integrate it with the prototype TOF system.

6.3. *DESIGN UPDATES*

6.3.1. Resources

	Last Month	This Month	Change
Mass (g) *	1336	1336	0
Power (mW)	1354	1354	0
Telemetry (bps)	418	418	0

* Includes 200g bookkept by GSFC for SIT structure

6.4. *OUTSTANDING PROBLEMS*

6.5. *NEW PROBLEMS*

6.6. *NEW RISKS*

6.7. *PROBLEM/FAILURE QUICK LOOK*

Starts at first turn-on of flight hardware.

ID #	Description	Assignee	Opened	Closed

7. CESR (SWEA) Status

CESR- TOULOUSE- FRANCE **Author : Claude Aoustin / Project Manager**

SWEA PROGRESS REPORT # 8
(May 14, 2002)

April 2002

CESR is in charge of :

- Electrostatic analyzer with deflectors, grids and Retractable Cover
- Detector consisting of two MCP rings
- Amplifiers and discriminators
- 3 High voltages

7.1. *Summary of Status*

Mechanical design end 17/12/2001 completed
Mechanical analyzer fabrication end 22/04/2002
Quite finished for the ETU (99 % done)
Electronics fabrication end mid April started (60 % done)
ETU Assembly start 17/06/2002 end 07/2002
Delivery to UCB was planned for 12/07/2002 : will be delayed !

7.2. *Major accomplishments*

Mechanical fabrication:

- First EM analyzer and housing fabricated.
- Deflector grids fabrication: one set (2 grids) fabricated. Transparency lower than expected (75% per grid). Could be increased for the flight models if necessary by having bigger cells.
- Spheres treatment and black coating on the way.
- Integration will start in June. Delayed due to the difficulty to get the grids within the expected time.
- Verification under vacuum in July.

Electronics boards are designed. 2 of them are fabricated. The last one is under fabrication. We have got some delay due to difficulties to implement all the components on the HV board. Should be populated and tested by the end of May/beginning of June.

Pin Puller ordered. Should arrive soon.

7.3. *Design Updates*

Mass : 1040 g
Power : 446 mW min ; 662 mW max

7.4. *Outstanding Problems*

AMPTEKS amplifiers quality:
- additional burn in will be done : 1000h at 125°C on 10 pieces.
- pind testing will be done as well.

7.5. *New problems*

None

7.6. *Top Risks*

7.7. *Problem Failure Quick Look*

None

8. GSFC (MAG) Status

Nothing to report.

9. EPO at UCB

April STEREO/IMPACT EPO report-

Informal Education:
April was a big dissemination month for the Stereo EPO.
STEREO/IMPACT EPO was represented during the CAL-DAY, UCB yearly open house. The UC Campus estimated an attendance of 30,000, we estimate more than couple of thousand people stopped by at our booth at the UC Campus as demonstrated with the picture and about 100 people visited the SSL. We highlighted the STEREO Mission through the Poster and the glasses and distributed more than 100 posters and glasses.

Nahide Craig