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Subject: IMPACT Monthly Technical Progress Report, Contract NAS5-00133

Harry:

Enclosed is the monthly technical progress report for the STEREO IMPACT project for the month of February 2002.

Sincerely,

David Curtis
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CC:

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IMPACT Team

1. IMPACT Overview

This report is presented in sections by institution. Section 1 is an IMPACT Project Manager / System Engineer's overview.

1.1. *Contracting / Funding*

The current funding allotment is expected to last through March 2002. Because of pipe-line delays in the system through to the subcontractors (Caltech and UMd) it is important that IMPACT be funded somewhat in advance of expected spending.

We have negotiated a revised budget for the launch slip after a few iterations and some decreases in level of effort.

1.2. *Significant System-Level Accomplishments*

- Still working on parts screening issues (selecting contractors, developing details test specs), getting approvals
- Working operational & survival heater issues for SEP and SWEA (refining thermal models).
- Requested boom deployment heater power service from APL.
- Attended EMC committee. HVPS synchronization waivers for SWEA and SIT rejected. Working on synchronized designs for both, with resource costs to be forwarded to Project if significant.
- New Caltech, UCB, and SEPT schedules have been submitted separately.

1.3. *System Design Updates*

No significant changes.

1.4. *System Outstanding Issues*

- Non-NASA funded institutions PAIP is still not accepted by Project. We are attempting to find a compromise. ESTEC is working on a revised PAIP. CESR is considering accepting the UCB PAIP with the "at least as good as" wording used by SWAVES.
- Project desires for maintenance of an "integrated IMPACT schedule" (which Project is currently building from the existing schedules) will require extra effort. We are looking into possibilities at Berkeley and will provide Project with a proposal.
- The IMPACT boom is behind schedule. In order to meet the desire to have a fully qualified prototype by CDR, we will need to add some extra effort. We are looking into the possibilities and will provide a proposal to Project.
- PLASTIC desires a dedicated programmer to write the PLASTIC flight software that lives in the IDPU. The programmer who wrote the code for a similar instrument on Cluster will be available around the end of the year, and could take over the detailed PLASTIC software coding. We have provided a proposal to Project for this option.

1.5. *Top 10 Risks*

Top 10 risks are attached, same as last month. Note that on UCB21, the SEP VLSI design has been submitted to fab., and for UCB23, many non-standard parts are in screening.

IMPACT Top Ten Risks 3/2002

No.	Risk Item	Score	Mitigation	Mitigation Schedule						
				PDR	Bread-board Test	CDR	Sub-system Test	System Test	Env test	Early Orbit Test
UCB_5	IMPACT boom is a new design. Failure could affect Imager pointing requirements as well as boom-mounted instruments.	HIGH	Design for reliability. Early development and test to ensure reliability.	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH
UCB_21	Custom VLSI used in SEP may has schedule and cost risk	MEDIUM	Early development to prove design; use Amptek in place of VLSI in SIT (stll use VLSI in HET, LET)	MEDIUM	MEDIUM	LOW	LOW	LOW	LOW	LOW
UCB_18	LET Detectors from a new manufacturer	MEDIUM	Working with manufacturer on process	MEDIUM	MEDIUM	LOW	LOW	LOW	LOW	LOW
UCB_23	Non-standard parts qualification failure could impact delivery schedule	MEDIUM	Early parts selection and screening	MEDIUM	MEDIUM	LOW	LOW	LOW	LOW	LOW
UCB_15	GSFC Approval Requirements could delay instrument delivery or add cost	MEDIUM	Difficult to asses, history is mixed	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	LOW
UCB_4	The IDPU is a single point failure mechanisim for the IMPACT suite and	HIGH	IDPU is a simple, reliable system. Extra attention will be paid to ensuring its reliability	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH
UCB_13	IMPACT team is thin; loss of a critical	MEDIUM	Reassign work amongst team as and when required	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	LOW	LOW
UCB_11	Stringent EMI requirements may delay schedule is testing fails	MEDIUM	Careful design, early testing	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	LOW	LOW
UCB_1	ITAR restriction of information exchange with foreign CoIs may result in problems	MEDIUM	Various channels of communication have been found within the ITAR restrictions to allow adequate information flow. Some	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	LOW
UCB_2	Increasing documentation requirements distract key personnel from design tasks	MEDIUM	Negotiate documentation requirements to minimize impact	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	LOW

2. Berkeley Status

2.1. *Summary of Status*

The UCB schedule with updated status and a reworked boom schedule will be delivered separately.

2.2. *Major Accomplishments*

SWEA/STE:

- Efforts to reduce STE noise level proceeding at LBNL
- SWEA/STE schematics nearly ready for layout.

IDPU:

- Data Controller Board design complete and into layout.
- Data Controller Board FPGA in work.

LVPS/HVPS:

- LVPS breadboard in test.

Boom:

- Thermal model proceeding (with Eby).
- Prototype boom fine-tuning complete, tests in progress

GSE:

- IDPU Simulator hardware working with UCB host PC software, in debug.

2.3. *Design Updates*

None

2.4. *Outstanding Problems*

- Operational heater power budget over allocation

2.5. *New Problems*

None.

2.6. *Top Risks.*

No new risks identified.

2.7. *Problem/Failure Quick Look*

None.

3. GSFC (SEP) Status

STEREO/IMPACT/SEP/GSFC Progress Report for February, 2002 – (von Rosenvinge, Baker, Hawk, Reames, Shuman, Wortman)

3.1. *Summary of Status*

Mostly on-schedule. The L1 detector mounts have been received and sent for mechanical inspection. A sample mount has also been sent to the detector manufacturer (Micron) for their approval. The HET H1 detector mount design is now 75% complete and the HET H3 mount is 50% complete. The L2 and L3 mounts are not started as of yet.

A meeting was held with the SIT team, including Co-Investigators from Germany, and the design of the electronics mechanical configuration and outline drawings have been started (~ 50% complete).

Since many of the SIT telescope parts are heritage parts, we are starting to submit drawings for fabrication. Six mechanical pieces for SIT were recently sent out for fabrication to flight vendors for 4 week delivery.

We are proceeding on the assumption that the UCB Low Voltage Power Supply will provide separate low voltage windings for SEPT.

3.2. *Major Accomplishments*

Worked on defining HET GSE software and hardware requirements. The HET GSE is being designed such that the GSE can be at Goddard and operate HET via TCP/IP sockets wherever HET is located (Goddard, Caltech, or APL). Preliminary HET energy bins were defined for on-board software processing and a format for transmitting HET pulse height data was defined.

Worked on detector mount designs as discussed earlier.

Completed some additional IMPACT/SEP PDR RFA responses.

3.2.1. Next month-

- Resolve Contamination Control issue re surface cleanliness at delivery.
- Work on completing detector mount designs.
- Work on preliminary design of SIT High Voltage Power Supply box.
- Complete preliminary packaging design for the SIT electronics.

3.3. *Design Updates*

None identified this month.

3.4. *Outstanding Problems*

Contamination Control: We have previously stated our plan to deliver our instruments with the exterior surfaces cleaned to level 500 B. This is in conflict with the requirement presented by APL calling for level 300 A. This still needs to be resolved.

3.5. *New Problems*

None.

3.6. *Top Risks*

No significant risks at GSFC? Need to ensure that manpower becomes available per the current plan.

3.7. *Problem/Failure Quick Look*

Kiel (SEPT) Status
SEPT Monthly Technical Progress Report
February 2002

3.8. *Summary of Status*

1. SEPT Telescope – Canberra delivered prototype detector stack. Incoming inspection started. Agreed on far field measurement with IMPACT/MAG in April 2002.
2. Sensor and E-Box Housing – Finished machining of test mount to hold the magnets. Finished machining of mock-up for E-Box.
3. SEPT Electronics – Significant progress in assembly of electronics boards, in software development and testing of electronics at ESTEC and at contractor site.
4. Manpower – Progress at ESTEC both internal (new staffing) and external (contracting out). Progress at Kiel: new position of scientist for SEPT filled: Dr. Stephan Boettcher.

3.9. *Major Accomplishments*

1. First SEPT solid state detector stack delivered (prototype). Incoming inspection in progress. Preliminary results: energy resolution OK, light tightness not OK, but light path for prototype model not yet representative for flight model! Investigations continue.
2. Finished machining of test mount for magnets. Agreement reached with Mario Acuna to measure far field at GSFC, cancelling our original plan to measure stray field at Technical University of Braunschweig, Germany.
3. Finished machining of mock-up for E-Box to serve as template for PCB mounting at ESTEC. Reached agreement to replace coax bias connector and 25-pin MDM connector by 31-pin MDM connector with TSQ for bias. This might make existing mock-up box obsolete. Design update in progress.
4. Digital board (DB)
    a. DB fully assembled – working (DAC, SRAM, FPGA, interface)
    b. DB-calibration circuit (not yet fully tested)
    c. Interface PC- SEPT working (minor technical problems to solve like split speed 9.6 kBaud.56.7 kBaud)
    d. SEPT commander (test software for emulating SEP DPU and testing of SEPT-SEP -communication is working
    e. Simulator (Visual Basic application) of FPGA is working
5. Analog Board (AB)
    a. PDFE's not mounted yet, rest is fully assembled
    b. Not yet tested – next in the loop.
    c. HS is in progress to develop software for the AB-Test Board
    d. Update of schematic done (include current read out)
6. AB-Test Board
    a. Fully assembled, under test now
    b. Has a few lines missing (2 serial lines) – can be repaired by hand wiring and use of spare pins
7. EGSE computer
    a. Plug in cards working, software in progress
    b. EGSE allows tuning every parameter of the FPGA and Analog part and display data in real time = growing product (parts are included when needed)

8. Components and parts
    a. FPGA's ordered (major part 60k€), paper work done (export license o.k.)
    b. Part list update done
9. Contracts
    a. Hans Smit (SW-contractor) working since Jan-02 - very productive!
    b. KTH fully deployed. Kick-off in January 02.
    c. Electronic boards, test equipment and computer delivered to them. Should start to think about phase II of the contract.
    d. Web cam with live image transmission installed (exchange of scope picture, data read,…). Access via ICA client to SEPT-EGSE in Sweden.
    e. Gaisler (contract delivered). Signature on Gaisler side is missing, but in progress. Reading contract, short before signature. We can kick-off in week 11
10. Manpower deployment
    a. Hans S. – 40% fully working.
    b. KTH contractor – fully working.
    c. Gaisler (Sandi) in waiting position.
    d. DK not yet full deployed / agreement and plans are in place.
    e. PF 20 %, BJ.
    f. New TM in negotiation (start 07/2002) PF-replacement.
    g. JH and BB are supporting.
11. PA/QA
    a. US-team needs input for PAIP update.
    b. US asked to sign WIND PA-plan – not possible, several items are different.
    c. Need to write own PA-plan -> Bengt Johlander.
    d. Testing of components- next steps (until end of year). Buy the COTS in bigger numbers.
    e. Make test board (together with current monitor and current limiter) – in progress.
    f. Radiation test CO-60 1,2,3,4,5,6,7,8,9,10, 15 krad CO-60 in planning.
    g. Proton facility test (latch-up behaviour) in planning
    h. Thermal stressing (all parts are in extended temperature range –40°C to +85°C) only on board level foreseen.
    i. US (Dave Curtis) offered possible help in screening (US-$ from NASA).
12. Planned activities for March 2002:
    a. Continue electrical incoming inspection of first detector stack.
    b. Order SRAM, connectors, triax cables, EMC board, commercial components.
    c. Parts list: indicate backup-solution for parts.
    d. PA-plan.
    e. Current Limiter circuit.
    f. Component testing (CO-60, proton) preparation.
    g. Integration AB + SSD-detectors (Kiel) // mid April?
    h. Documentation (TM together with PF, BJ,DK,HS,TS,RM).
    i. Pin out of cabling.
    j. EM – PCB development should start soon.

3.10. *Design Updates*

1. Replacement of Triax-connector (Bias) and 25-pin MDM connector (telemetry, power) by one 31-pin MDM connector with TSQ for bias.

3.11. *Outstanding Problems*

3.12. *New Problems*

3.13. *Top Risks*

3.14. *Problem/Failure Quick Look*

4. Caltech/JPL (SEP) Status

February 2002

4.1. *Summary of Status*

Activities centered on the VLSI design and submission for fab, electronics development, detector development, the SEP Software, GSE Software, and re-planning/re-budgeting.

4.2. *Major Accomplishments*

Schedule development:

- A new schedule/budget was produced (LET.SEP.BCDE.2.26.02.mpp) in order to slash $800K from the 12.14.01 budget through Phase D. Among the casualties of the new budget are all the SEP internal team meetings, save one. Also, Caltech will be joining the weekly SEP team conference calls every other week. Other travel was affected; in general only one Co-I from Caltech/JPL is budgeted for the SWG meetings. No one from Caltech/JPL will attend the Paris SWG and conference due to budgetary considerations. There were many other changes too numerous to mention. In the process of re-budgeting and re-planning, the schedule reserve was decreased from 10.2 weeks to 7.7 weeks. The Phase E budget was also decreased and there is now very little funding in FY08. The Project has agreed to fix this deficiency at a later date. The budget is very tight with no reserve being kept at Caltech.

Electronics:

- The layout for the VLSI was submitted to AMI on 2/27/02. The chips are expected back in 10-12 weeks.
- Drafted ASIC hybrid screening specification. It will be reviewed by a hybrid parts specialist at either GSFC or JPL next month.
- Updated SEP power flow and sent it to LVPS designer at UCB.
- Updated ICD connector pinout and harness. Identified areas where mass resources are overspent (e.g., due to strict EMC/EMI requirements) but could be trimmed down by different choice of connector and wire. We are still working on those items.
- Initiated test lead-forming on dummy Actel parts.

GSE:

- Added software to compensate for gear backlash in the stage movement for the Detector Development System.
- Updated the programmer/user's guide for the stage movement software to reflect the new software.

Software:

- Wrote 1st draft of LET and SEP-Central software requirements document.
- Worked on LET onboard-processing algorithms for recording look-direction information.

Detectors:

- The first 2 of the 10 L1 wafers that have had front-side patterning done by Micron Semiconductor have been sent to JPL for thinning. This is the first attempt at thinning silicon wafers that could potentially yield functioning L1 detectors. The thinning work has been started.
- Micron Semiconductor has started production of the first batches of silicon wafers for making the H1+L3, L2, and H3 detectors (quantities of wafers: 4, 4, and 2, respectively). They have also started the manufacturing of a new jig needed for ion implanting the L2 wafers.
- Software for controlling thickness scans of L1 detectors using alpha-particles has been written and successfully tested operating mechanical positioners for the test system at JPL.

4.3. *Design Updates*

- No changes to mass and power estimates.

4.4. *Outstanding Problems*

None.

4.5. *New Problems*

None.

4.6. *Top Risks.*

- The budget is very tight with no reserve being held at Caltech. In addition, small increments of funding covering short time periods threatens our development schedule. We are constantly having to stop and re-start work at JPL. We need larger amounts of funding covering longer time periods (years).
- Schedule slack that we show explicitly will be taken away from us.
- Development of the L1 detector. (See September report for details.) Risk mitigated by creating slack in schedule and by starting a parallel development effort using different and more conventional manufacturing technique.
- Development of the VLSI chip. (See September report for details.) Risk mitigated by providing for two more months for the layout and checking while still keeping 30 weeks for a second run if necessary.

4.7. *Problem/Failure Quick Look*

None.

5. SIT MONTHLY TECHNICAL PROGRESS REPORT

February 2002

5.1. *SUMMARY of STATUS*

a. SIT TELESCOPE -Thermal design is in work. Prototype is in house and working.

b. SIT TOF System - Flight modifications to Prototype electronics design and layout are underway.

c. SIT Energy/Logic System - Energy system is being redesigned with Amptek parts. Preliminary design completed and prototype layout. Waiting for PC Board.

d. SIT HVPS - HVPS box drawing (exterior details only) generated by GSFC.

5.1.1. Schedule Changes

None

5.2. *MAJOR ACCOMPLISHMENTS*

5.2.1. This Month

TOF - We had a meeting of UMd personnel, Axel Korth and Klaus Heerlein of MPAe, Christian Dierker of TUB and Sandy Shuman of GSFC to discuss the TOF system. A proposed flight layout of the analog TOF electronics was presented and tested with the prototype telescope and found to work well. Packaging was discussed, connectors decided on and issues of board spacing, and connector and mounting hole location tentatively worked out. Sandy was tasked with generating a drawing showing how everything would fit in his box and specifying mounting/connector locations exactly. When this is done, final layouts can be generated.

Energy - Prototype design for the energy system using Amptek hybrids was generated and a prototype layout was prepared and submitted to a PC house. We expect prototype boards in mid March. Amptek parts have been ordered for the prototype.

HVPS - The HVPS box drawing (exterior details only) was generated by Sandy at GSFC

Software - the preliminary SIT Flight Software requirements document was prepared and submitted to Tycho at GSFC.

5.2.2. Next Month

We will design and implement the logic necessary to test the energy electronics in a Xilinx prototyping board. Along with this we will need to change the existing GSE software to handle both the prototype TOF and energy systems.
We expect to assemble the prototype energy electronics. When all of this is accomplished we will begin testing

We owe GSFC an update of the front-end logic requirements document including the new energy design. This will be generated when we have verified that our energy GSE works.

5.3. ***DESIGN UPDATES***

5.3.1. Resources

	Last Month	This Month	Change
Mass (g) *	1336	1336	0
Power (mW)	1354	1354	0
Telemetry (bps)	418	418	0

* Includes 200g bookkept by GSFC for SIT structure

5.4. ***OUTSTANDING PROBLEMS***

5.5. ***NEW PROBLEMS***

5.6. ***NEW RISKS***

5.7. ***PROBLEM/FAILURE QUICK LOOK***

Starts at first turn-on of flight hardware.

ID #	Description	Assignee	Opened	Closed

6. CESR (SWEA) Status

CESR- TOULOUSE- FRANCE **Author : Claude Aoustin / Project Manager**

SWEA PROGRESS REPORT # 6
(March 14, 2002)

February 2002

CESR is in charge of :

- Electrostatic analyzer with deflectors, grids and Retractable Cover
- Detector consisting of two MCP rings
- Amplifiers and discriminators
- 3 High voltages

6.1. *Summary of Status*

Mechanical design end 17/12/2001 completed
Mechanical analyzer fabrication end 22/04/2002 started (85 % done)
Electronics fabrication end mid April started (30 % done)
ETU Assembly start 06/05/2002 end 05/07/2002
Delivery to UCB 12/07/2002

6.2. *Major accomplishments*

Mechanical fabrication :

- First EM analyzer and housing fabricated,
- Deflector grids fabrication on the way,
- Due to the lack of the Pinpuller (available mid-April), a dummy top hat fixation will be fabricated to allow analyser response verification.
- Spheres treatment and black coating will start end of March and will be finished around the 10 of May.
- Integration will start mid May.
- Verification under vacuum end of May.

Deflectors grids fabrication on the way.

Electronics boards are designed. Resistors added on the MCP board for heating purpose. Fabrication of the 3 electronics boards on the way.
Should be populated and tested by the end of April.

Pin Puller ordered.

6.3. *Design Updates*

Mass : 1040 g
Power : 446 mW min ; 662 mW max

6.4. *Outstanding Problems*

Mechanical design has been finalized taking into account the Pin Puller information, purging system position and UCB section interface.

Grids added over the MCPs.

To be in compliance with the EMC and electromagnetic cleanliness, we are studying how to add crystal control on HV. For the first EM the HV will not be synchronised.

AMPTEKS amplifiers quality
It will difficult for us to have the best quality for them as done for Goddard

6.5. *New problems*

None

6.6. *Top Risks*

6.7. *Problem Failure Quick Look*

None

7. GSFC (MAG) Status

Nothing to report