Harry Culver, Code 740.1
STEREO IMPACT Instrument Manager
Goddard Space Flight Center
Greenbelt, MD. 20771

Subject: IMPACT Monthly Technical Progress Report, Contract NAS5-00133

Harry:

Enclosed is the monthly technical progress report for the STEREO IMPACT project for the month of January 2002.

Sincerely,

David Curtis
IMPACT Project Manager
University of California, Berkeley

CC:

Loren.M.Kruger.1@gsfc.nasa.gov
Claudia.Krogel.1@gsfc.nasa.gov
Harry.Culver@gsfc.nasa.gov
IMPACT Team

# 1. IMPACT Overview

This report is presented in sections by institution. Section 1 is an IMPACT Project Manager / System Engineer's overview.

## 1.1. *Contracting / Funding*

The current funding allotment is expected to last through March 2002. Because of pipe-line delays in the system through to the subcontractors (Caltech and UMd) it is important that IMPACT be funded somewhat in advance of expected spending.

We have received (early January) two contract mods from Project; one with a new SOW and one with a new launch date. We are working on a corresponding revised budget.

## 1.2. *Significant System-Level Accomplishments*

- Still working on parts screening issues (selecting contractors, developing details test specs), getting approvals
- Working operational & survival heater issues for SEP and SWEA (refining thermal models); also estimated mass (heaters were not in previous mass estimates). Note a recent decrease in the SEA operational heater requirement.
- Collecting data for EMC waiver request EMC3 (unsynchronized converters)
- Decided on Amptek solution for SIT front end (replaces VLSI). Simplifies the SIT development plan and reduces risk at the cost of some small mass and power growth (partially offset by decrease in SIT TOF power).
- New mass estimate for SEP LVPS with separate secondary windings for SEPT to meet EMC requirements. About 350g growth, including increased SEP-Common box size.

## 1.3. *System Design Updates*

Mass and power spreadsheet update submitted separately (and provided to APL). Several small changes as noted above.

## 1.4. *System Outstanding Issues*

- Non-NASA funded institutions PAIP is still not accepted by Project. We are attempting to find a compromise.

## 1.5. *Top 10 Risks*

Top 10 risks are attached, same as last month. The project risk management database is still inaccessible.

IMPACT Top Ten Risks 1/2002

| No. | Risk Item | Score | Mitigation | Mitigation Schedule | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | PDR | Bread-board Test | CDR | Sub-system Test | System Test | Env test | Early Orbit Test |
| UCB_5 | IMPACT boom is a new design. Failure could affect Imager pointing requirements as well as boom-mounted instruments. | HIGH | Design for reliability. Early development and test to ensure reliability. | HIGH | HIGH | HIGH | HIGH | HIGH | HIGH | HIGH |
| UCB_21 | Custom VLSI used in SEP may has schedule and cost risk | MEDIUM | Early development to prove design; use Amptek in place of VLSI in SIT (stll use VLSI in HET, LET) | MEDIUM | MEDIUM | LOW | LOW | LOW | LOW | LOW |
| UCB_18 | LET Detectors from a new manufacturer | MEDIUM | Working with manufacturer on process | MEDIUM | MEDIUM | LOW | LOW | LOW | LOW | LOW |
| UCB_23 | Non-standard parts qualification failure could impact delivery schedule | MEDIUM | Early parts selection and screening | MEDIUM | MEDIUM | LOW | LOW | LOW | LOW | LOW |
| UCB_15 | GSFC Approval Requirements could delay instrument delivery or add cost | MEDIUM | Difficult to asses, history is mixed | MEDIUM | MEDIUM | MEDIUM | MEDIUM | MEDIUM | MEDIUM | LOW |
| UCB_4 | The IDPU is a single point failure mechanisim for the IMPACT suite and | HIGH | IDPU is a simple, reliable system. Extra attention will be paid to ensuring its reliability | HIGH | HIGH | HIGH | HIGH | HIGH | HIGH | HIGH |
| UCB_13 | IMPACT team is thin; loss of a critical | MEDIUM | Reassign work amongst team as and when required | MEDIUM | MEDIUM | MEDIUM | MEDIUM | MEDIUM | LOW | LOW |
| UCB_11 | Stringent EMI requirements may delay schedule is testing fails | MEDIUM | Careful design, early testing | MEDIUM | MEDIUM | MEDIUM | MEDIUM | MEDIUM | LOW | LOW |
| UCB_1 | ITAR restriction of information exchange with foreign CoIs may result in problems | MEDIUM | Various channels of communication have been found within the ITAR restrictions to allow adequate information flow. Some | MEDIUM | MEDIUM | MEDIUM | MEDIUM | MEDIUM | MEDIUM | LOW |
| UCB_2 | Increasing documentation requirements distract key personnel from design tasks | MEDIUM | Negotiate documentation requirements to minimize impact | MEDIUM | MEDIUM | MEDIUM | MEDIUM | MEDIUM | MEDIUM | LOW |

# 2. Berkeley Status

## 2.1. *Summary of Status*

A new UCB schedule with updated status was delivered in January.

## 2.2. *Major Accomplishments*

SWEA/STE:

- Improved thermal model reduces SWEA operational heater requirements
- Prototype STE door actuator in fab.
- Efforts to reduce STE noise level proceeding at LBNL
- STE sensor significantly reduced in size by removing most of the electronics to near by boxes. Allows STE sensor to run colder which should improve noise.

IDPU:

- Elf subcontract to design of Data Controller Board set up. Elf has generated first design description documents in response to the specification provided by UCB.

LVPS/HVPS:

- Measured HESSI HVPS EMC (CE) for SIT HVPS synchronization waiver.
- SIT HVPS ETU transformer in work
- SIT HVPS Form factor decided on
- LVPS breadboard in work.

Boom:

- Thermal model proceeding (with Eby).
- Prototype boom fine-tuning in progress

GSE:

- IDPU Simulator hardware working with UCB host PC software, in debug.

## 2.3. *Design Updates*

None

## 2.4. *Outstanding Problems*

- SWEA operational heater estimate needs refining based on a better thermal model. Possible modest increase in heater power requirement.
- SWEA/STE mass needs to be re-estimated based on new configuration

## 2.5. *New Problems*

None.

## 2.6. *Top Risks.*

No new risks identified.

## 2.7. *Problem/Failure Quick Look*

None.

# 3. GSFC (SEP) Status

STEREO/IMPACT/SEP/GSFC Progress Report for January, 2002 – (von Rosenvinge, Baker, Hawk, Reames, Shuman, Wortman)

## 3.1. *Summary of Status*

Mostly on-schedule. The L1 mount has been ordered and completed mounts are expected in late February. The decision to not use the Caltech VLSI chip in SIT was made and we are waiting for the new front-end interface for SIT to be specified by UofMD. UCB may require a significant volume/weight change for the Low Voltage Power Supply if SEPT is to have separate low voltage windings. We are awaiting a decision. Requirements for operational and survival heaters have been determined. Estimates of the weight and power impacts of all these items have been determined.

## 3.2. *Major Accomplishments*

- Worked on the SEP thermal design and determined the power needed for operational and survival heaters.
- Worked on defining HET software and hardware requirements; wrote prototype HET on-board code.
- Completed IMPACT/SEP PDR RFA responses.
- Completed preliminary HET software requirements document.
- Completed initial SEP thermal design.

### 3.2.1. Next month

- Resolve Contamination Control issue re surface cleanliness at delivery.
- Work on H1, H3 and L3 detector mount designs.
- Work on preliminary design of SIT High Voltage Power Supply box.
- Work on packaging SIT electronics.

## 3.3. *Design Updates*

Weight and power deltas associated with heaters, the UofMD decision to not use the Caltech ASIC, and the increased size of the Low Voltage Power Supply have been discussed with Caltech and Caltech has forwarded these to Berkeley.

## 3.4. *Outstanding Problems*

Contamination Control: We have previously stated our plan to deliver our instruments with the exterior surfaces cleaned to level 500 B. This is in conflict with the requirement presented by APL calling for level 300 A. This needs to be resolved.

## 3.5. *New Problems*

George Winkert did not become available to work on the SIT front-end electronics according to plan. We have reviewed this situation and he will become available approximately March 8. This will be soon enough for George to meet his commitments. Larry Ryan's availability also became an issue and has been resolved satisfactorily.

## 3.6. *Top Risks*

# 4. Kiel (SEPT) Status

**SEPT Monthly Technical Progress Report**
**January 2002**

## 4.1. *Summary of Status*

1. SEPT Telescope – Finished implementing the design changes resulting from SEPT Team Meeting in November 2001. Further delay of detector stack delivery from Canberra. New delivery date: 2nd half of February 2002.
2. Sensor and E-Box Housing – Finished updating the mechanical drawings. Started machining of test mount to hold the magnets. Started machining of mock-up for E-Box.
3. Testing of electronics boards in progress. Software development for FPGA simulator in progress.
4. Manpower – Progress at ESTEC both internal (new staffing) and external (contracting out). Progress at Kiel: hiring process finished for new position as scientist.

## 4.2. *Major Accomplishments*

1. Continued discussion on op-heaters and non-op heaters. Decision: splice out heater harness.
2. Started machining of test mount for magnets. This mount is used for stray field measurements to be carried out at Technical University of Braunschweig, Germany.
3. Started machining of mock-up for E-Box. This box serves as template for PCB mounting at ESTEC.
4. Manpower and contract deployment at ESTEC:
    a. Contract with KTH signed. Kick off on 10.&11. January. Analog Board + Digital Board + Test Bench + EGSE computer transferred. Test of electronics boards in progress. Reports of test results are being generated to serve as input for the next iteration of the boards (EM). Contract duration of phase 1: 4 months, and phase 2: 8 months.
    b. In-house contractor 50% FTE for software development working on EGSE and test software, hired since 02-JAN-02.
    c. Contract with Gaisler Research signed. Kick-off in the next weeks. This contract is for the next integration (hopefully the FM) of the SEPT FPGA, duration: 8 months.
    d. Senior engineer 25% FTE for SEPT since January 2002 in place. Task allocation in progress.
    e. Peter Falkner running on 20% FTE (sorry).
    f. Job interview with new project manager for SEPT (50% FTE) done. Pending okay from candidate.
5. FPGA is working (not all functions are tested yet). Communication FPGA - EGSE (PC) is working. EGSE software under development. User manual in preparation.
6. FPGA simulator (=SEPT simulator) in progress (all functions already implemented). This PC-program simulates the behavior of SEPT FPGA and is able to receive all commands via RS-232 and replies with SEPT data like a real FPGA according to FPGA data sheet issue 1. This may be of interest to CalTech for their software development.

7. Analog and digital board testing in progress.
8. Planned activities for February 2002
    a. Finish machining of magnet housing, finish machining of mock-up for E-Box, incoming inspection of first detector stack.
    b. Continue discussion on harness: there is a lack of redundancy in 25-pin connector and bias line between SEPT and SEP. Decision to be made between 25 pin and 31 pin MDM connector. Decision to be made between coax cable (or rather triax RG403) and TSQ for bias.
    c. Continue board testing and software development for EGSE and SEPT simulator.

## 4.3. *Design Updates*

1. Change of connector type of 13 coax connectors for signals between sensor and E-box: Original type: SSMC microminiature coaxial for RG179, new type: NDL-T miniature triaxial for RG403. Rationale: As we have no control over the MLI design, the connectors might face open space. As coax are on analog ground, we would expose the sensitive analog ground to solar wind or arcing from charged surfaces nearby. Triax connectors avoid this EMI problem.
2. This may apply also for the bias cable from SEP to SEPT in case we decide against TSQ.

## 4.4. *Outstanding Problems*

1. Lack of redundancy in harness (25-pin MDM and triax NDL-T) between SEPT and SEP. Decision pending between 25-pin and 31-pin for telemetry/power, and between triax and TSQ (twisted shielded quad) wires for bias.

## 4.5. *New Problems*

## 4.6. *Top Risks*

## 4.7. *Problem/Failure Quick Look*

# 5. Caltech/JPL (SEP) Status

January 2002

## 5.1. *Summary of Status*

Activities centered on the VLSI design, electronics development, detector development, the SEP Software, and GSE Software.

## 5.2. *Major Accomplishments*

Electronics:

- Focus remains on the layout and checking of the PHA VLSI chip. The "core" consisting of 16 complete dual-gain PHAs including digital back sections has been completed and checked with both Gemini and Tanner LVS (layout versus schematic) tools. The core has been inserted into the padframe and is presently being wired to the peripheral circuitry. Remaining pre-submission tasks include
    - complete chip LVS,
    - digital simulation check from layout using IRSIM
    - analog SPICE simulation check using schematics known to match layout..
- Obtained favorable quote from AMI for VLSI wafer fabrication in the same discounted amount (77.5 k$) as previously negotiated on HEFT project.
- Obtained quote from JPL for ASIC hybrid fabrication.
- Made contacts with manufacturers of flight heaters (Tayco Engineering), connectors (Nanonics) and chip thermistors.
- Received order of flight chip resistors from Mini-Systems, to be used in the ASIC hybrid.
- Provided EMI test reports from ACE mission to UCB for waiver consideration on SEP SSD Bias Supply.
- Included heater hardware mass estimates in the resources table which is attached. Also updated mass estimates for SEPT harness, LVPS, LET shield and SIT. Updated power estimate due to addition of +/- 6V for SIT.

GSE:

- Finished the stage movement software for the Detector Development System.
- Partially tested stage movement software (hardware is not fully assembled).
- Wrote a programmer/user's guide for the stage movement software.

Software:

- Gathered inputs from SEP team members for LET and SEP-Central software requirements docs.

- Worked on LET onboard-processing algorithms for recording look-direction information.

Detectors:

- Tests of the process being used by JPL for thinning sections of Si wafers for making the 20 micron thick L1 detector continued. It was found that using a high-molarity

KOH etchant produces much better surface smoothness than etchants perviously tried. A test wafer etched in this way using the L1 etch-mask was completed and the thickness uniformity measured at Caltech. Three of four thinned areas had absoulte thicknesses within the specified range (18-22 microns), and all had good thickness uniformity.

- Micron Semiconductor, the detector manufacturer, has completed the front-side patterning of 10 Si wafers with the L1 pattern and is holding them until needed for thinning by JPL.

- In consultation with Micron Semiconductor, it was decided that we are ready for the first test of thinning Si wafers that have the front-side detector patterning in place. Micron will send two of the wafers that they processed to JPL for this purpose.

- An order was placed with Micron Semiconductor to produce prototype L1 detectors made from 20 micron thick Si wafers rather than from thick wafers that have been etched thin only in the areas to be occupied by the detectors. This activity is being carried out as a backup to the baseline thick/thin approach in order to mitigate risk.

### 5.3. *Design Updates*

- Mass and power update sent separately.

### 5.4. *Outstanding Problems*

None.

### 5.5. *New Problems*

None.

### 5.6. *Top Risks.*

- Small increments of funding covering short time periods threatens our development schedule. We are constantly having to stop and re-start work at JPL. We need larger amounts of funding covering longer time periods (years).
- Schedule slack that we show explicitly will be taken away from us.
- Development of the L1 detector. (See September report for details.) Risk mitigated by creating slack in schedule and by starting a parallel development effort using different and more conventional manufacturing technique.
- Development of the VLSI chip. (See September report for details.) Risk mitigated by providing for two more months for the layout and checking while still keeping 30 weeks for a second run if necessary.

### 5.7. *Problem/Failure Quick Look*

None.

# 6. SIT MONTHLY TECHNICAL PROGRESS REPORT

January 2002

## 6.1. *SUMMARY of STATUS*

a. SIT TELESCOPE -Thermal design is in work. Prototype is in house and working.
b. SIT TOF System - Prototype TOF electronics is fully designed and is in test.
c. SIT Energy/Logic System - Energy system is being redesigned with Amptek parts
d. SIT HVPS - Interconnection between telescope and HVPS worked out. HVPS box drawing (exterior details only) due to UCB from GSFC.

### 6.1.1. Schedule Changes

The schedule was recast for the new energy system. The format is such that slack can be determined and the new schedule was submitted to Harry Culver at GSFC. The current schedule is dated 1/30/02.

## 6.2. *MAJOR ACCOMPLISHMENTS*

### 6.2.1. This Month

TOF - We completed testing of the prototype TOF system with the telescope and alpha particles. Good performance was achieved, even slightly better than we had using the lab digital electronics last year. A couple of desired small design changes were found and a need to increase the maximum TOF from 60ns to 102 ns was identified. Given the wider TOF range we also found we need to increase the resolution of the TOF system from 8 to 9 bits. These items were discussed with the designer at TUB and the necessary hardware changes are being incorporated in the digital system. We expect to test the modified design next month.

Energy - after discussions among the co-Is and some refining of the estimates for the mass and power increases necessary, we were given the go-ahead to develop an Amptek hybrid-based design for the SIT energy system to replace the design using the Caltech ASIC. This will free us up to proceed immediately with energy system design, and this effort has in fact begun. We have also been able to widen the electronics operating temperature limits for the SIT electronics as a result of this change and we are hopeful that this will result in a smaller operational heater for SIT.

HVPS - a teleconference between GSFC, UCM and UMd resolved that instead of using HV connectors, the UCB-supplied SIT HVPS will be shipped with HV wires attached and these will be connected to the telescope at GSFC during telescope assembly. The HV supply box size was determined and Sandy Shuman a GSFC was tasked with generating a design of the exterior of the HV box.

### 6.2.2. Next Month

We have a scheduled visit from the TOF designers from TUB and MPAe the week of Feb 18. For this meeting we need to make the changes in the TOF GSE needed to support the modified TOF hardware. Also attending will be Sandy Shuman from GSFC to resolve any remaining mechanical design issues. We expect to freeze the TOF design after this visit.

After the TOF is resolved we will work on the energy design.

## 6.3. *DESIGN UPDATES*

### 6.3.1. Resources

| | Last Month | This Month | Change |
|---|---|---|---|
| Mass (g) * | 1220 | 1336 | 116 |
| Power (mW) | 1349 | 1354 | 5 |
| Telemetry (bps) | 418 | 418 | 0 |

* Includes 200g bookkept by GSFC for SIT structure

Mass increased from the addition of an Amptek energy board to the electronics and the associated increase in supporting items.
Power increased from the switch from the Caltech chip to the Amptek design, but decreased from the reporting of actual measured power for the TOF system in place of the estimates we had been carrying. The result was a 5 mW increase.

## 6.4. *OUTSTANDING PROBLEMS*

## 6.5. *NEW PROBLEMS*

## 6.6. *NEW RISKS*

## 6.7. *PROBLEM/FAILURE QUICK LOOK*

Starts at first turn-on of flight hardware.

| ID # | Description | Assignee | Opened | Closed |
|---|---|---|---|---|
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |

# 7. CESR (SWEA) Status

**CESR- TOULOUSE- FRANCE** **Author : Claude Aoustin / Project Manager**

## SWEA PROGRESS REPORT # 5
## (February 14, 2002)

January 2002

CESR is in charge of :
- Electrostatic analyzer with deflectors, grids and Retractable Cover
- Detector consisting of two MCP rings
- Amplifiers and discriminators
- 3 High voltages

### 7.1. *Summary of Status*

- Mechanical design end 17/12/2001 completed
- Mechanical analyzer fabrication end 22/04/2002 started
- Electronics fabrication end 28/01/2002 started
- ETU Assembly start 06/05/2002 end 05/07/2002
- Delivery to UCB 12/07/2002

### 7.2. *Major accomplishments*

- Mechanical fabrication has started.
- Deflectors grids fabrication on the way.
- Electronics boards are designed. Resistors added on the MCP board for heating purpose. Fabrication of the 3 electronics boards started.
- Pin Puller ordered.

### 7.3. *Design Updates*

Mass : 1040 g

Power : 446 mW min ; 662 mW max

### 7.4. *Outstanding Problems*

- Thermal design : First results received
- Mechanical design has been finalized taking into account the Pin Puller information, purging system position and UCB section interface.
- Grids added over the MCPs.
- AMPTEKS amplifiers quality
    - It will difficult for us to have the best quality for them as done for Goddard

### 7.5. *New problems*

None

### 7.6. *Top Risks*

### 7.7. *Problem Failure Quick Look*

None

## 8. GSFC (MAG) Status

Nothing to report