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Subject: IMPACT Monthly Technical Progress Report, Contract NAS5-00133

Harry:

Enclosed is the monthly technical progress report for the STEREO IMPACT project for the month of December 2001.

Sincerely,

David Curtis
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CC:

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IMPACT Team

1. IMPACT Overview

This report is presented in sections by institution. Section 1 is an IMPACT Project Manager / System Engineer's overview.

1.1. *Contracting / Funding*

Caltech and UMd are just now under Phase B/C/D/E subcontract.

The current funding allotment has just about run out, and a new allotment is expected soon to last through March 2002. Because of pipe-line delays in the system through to the subcontractors (Caltech and UMd) it is important that IMPACT be funded somewhat in advance of expected spending.

We have received (early January) two contract mods from Project; one with a new SOW and one with a new launch date. We are working on a corresponding revised budget.

1.2. *Significant System-Level Accomplishments*

- Participated in Mission PDR at APL
- Held an IMPACT team meeting at Berkeley. Issues and status were discussed. IDPU Software Requirements were reviewed by the team.
- Held a SWEA meeting between UCB and CESR to refine details of interfaces
- Still working on parts screening issues (selecting contractors, developing details test specs), getting approvals
- Working operational & survival heater issues for SEP and SWEA (refining thermal models)
- Submitted waiver requests to EMC committee
- SEP has developed additional slack in their schedule, partially by delivering directly to APL instead of Berkeley.

1.3. *System Design Updates*

Mass and power spreadsheet update submitted separately (and provided to APL). No significant changes (heater requirements still open pending final results of thermal models)

1.4. *System Outstanding Issues*

- Problem with heaters – had planned external mounting, which violates EMC requirements. There will be some small mass impact in adding some kind of EMC shield.
- Non-NASA funded institutions PAIP is still not accepted by Project. We are attempting to find a compromise.
- Looking at adding protection to SEP LVPS so that a failure in one instrument will not propagate into the rest.
- The current design of low voltage power distribution violates the EMC requirements (due to the break-up of STE and SEP). We are working on estimating the resource costs required to fix the system to be compliant, and at the same time, investigating if a waiver would be possible. This change goes beyond just adding extra windings to

the LVPS – it affects the power distribution inside the SEP Central box, and the harness from SEP Central to the SEPT units.

1.5. *Top 10 Risks*

Top 10 risks are attached, same as last month. The project risk management database is still inaccessible.

IMPACT Top Ten Risks 12/2001

No.	Risk Item	Score	Mitigation	Mitigation Schedule						
				PDR	Bread-board Test	CDR	Sub-system Test	System Test	Env test	Early Orbit Test
UCB_5	IMPACT boom is a new design. Failure could affect Imager pointing requirements as well as boom-mounted instruments.	HIGH	Design for reliability. Early development and test to ensure reliability.	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH
UCB_21	Custom VLSI used in SEP may has schedule and cost risk	MEDIUM	Early development to prove design	MEDIUM	MEDIUM	LOW	LOW	LOW	LOW	LOW
UCB_18	LET Detectors from a new manufacturer	MEDIUM	Working with manufacturer on process	MEDIUM	MEDIUM	LOW	LOW	LOW	LOW	LOW
UCB_23	Non-standard parts qualification failure could impact delivery schedule	MEDIUM	Early parts selection and screening	MEDIUM	MEDIUM	LOW	LOW	LOW	LOW	LOW
UCB_15	GSFC Approval Requirements could delay instrument delivery or add cost	MEDIUM	Difficult to asses, history is mixed	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	LOW
UCB_4	The IDPU is a single point failure mechanisim for the IMPACT suite and	HIGH	IDPU is a simple, reliable system. Extra attention will be paid to ensuring its reliability	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH
UCB_13	IMPACT team is thin; loss of a critical	MEDIUM	Reassign work amongst team as and when required	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	LOW	LOW
UCB_11	Stringent EMI requirements may delay schedule is testing fails	MEDIUM	Careful design, early testing	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	LOW	LOW
UCB_1	ITAR restriction of information exchange with foreign CoIs may result in problems	MEDIUM	Various channels of communication have been found within the ITAR restrictions to allow adequate information flow. Some	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	LOW
UCB_2	Increasing documentation requirements distract key personnel from design tasks	MEDIUM	Negotiate documentation requirements to minimize impact	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	LOW

2. Berkeley Status

2.1. *Summary of Status*

Much of Berkeley's effort this month went into the Mission PDR and Team Meeting. No significant new schedule issues.

2.2. *Major Accomplishments*

SWEA/STE:

- Held a meeting between CESR and UCB to refine interfaces
- SWEA aperture characteristics provided to Thermal Analyst to help in determining operational heater required
- Prototype STE door actuator in fab.
- Efforts to reduce STE noise level proceeding at LBNL

IDPU:

- Flight Software Requirements / Implementation Review held
- Iterated mechanical design

LVPS/HVPS:

- Estimated board space requirements for new SEP LVPS with separate SEPT LVPS secondaries to meet EMC requirements.
- SIT HVPS ETU transformer in work
- LVPS topology redesigned to minimize use of non-standard parts. A breadboard shall be built next month.

Boom:

- Thermal model proceeding (with Eby).
- Prototype boom (2 segments) demonstrated at Mission PDR (still needs some fine-tuning).

GSE:

- IDPU Simulator hardware delivered to UCB and testing with host PC software drivers started.

2.3. *Design Updates*

None

2.4. *Outstanding Problems*

- SWEA operational heater estimate needs refining based on a better thermal model. Possible modest increase in heater power requirement.
- SWEA/STE mass needs to be re-estimated based on new configuration

2.5. *New Problems*

None.

2.6. *Top Risks.*

No new risks identified.

2.7. *Problem/Failure Quick Look*

None.

3. GSFC (SEP) Status

STEREO/IMPACT/SEP/GSFC Progress Report for December, 2001 – (von Rosenvinge, Baker, Hawk, Reames, Shuman, Wortman)

3.1. *Summary of Status*

Mostly on-schedule. The L1 mount design underwent one final iteration, resulting in a total schedule delay of ~2 1/2 months. Completed mounts are expected in late January. SIT may opt to not use the Caltech VLSI chip and UCB may require a significant volume/weight change for the Low Voltage Power Supply if SEPT is to have separate low voltage windings. We are awaiting decisions regarding these two items. Requirements for operational and survival heaters are not yet fully determined and are overdue.

3.2. *Major Accomplishments -*

Modified the LET mechanical design in order to better isolate the detectors from outgassing of electronics parts. This also provides improved electrical shielding of the detectors. Modified the L1 detector prototype mount design accordingly. The latter was important because it keeps open the option to fly prototype detectors.

Worked on the SEP thermal design to determine the power needed for operational and survival heaters. Still not complete.

Studied SIT front-end logic specification (received from UofMD Oct 15).

Worked on defining HET software and hardware requirements; wrote prototype HET on-board code.

Attended STEREO Observatory PDR at APL and IMPACT Team Meeting at UC Berkeley.

3.2.1. Next Month

- Complete IMPACT/SEP PDR RFA responses.
- Complete HET software requirements document.
- Complete SEP thermal design.
- Release updated schedule.
- Resolve Contamination Control issue re surface cleanliness at delivery.

3.3. *Design Updates*

Currently none. Expecting the size of the Low Voltage Power Supply to increase and requirements to emerge for operational and survival heaters. In addition, it had been expected that the survival heaters and thermostats would be applied externally by APL and that the associated weight would be charged to APL. It now appears that we are going to have to supply these ourselves and that they will need to be shielded for EMI reasons. There will be a corresponding weight penalty which has not yet been determined.

3.4. *Outstanding Problems*

Contamination Control: We have previously stated our plan to deliver our instruments with the exterior surfaces cleaned to level 500 B. This is in conflict with the requirement presented by APL calling for level 300 A. This needs to be resolved.

3.5. *New Problems*

No new problems.

3.6. *Top Risks*

No significant risks at GSFC?

3.7. *Problem/Failure Quick Look*

4. Kiel (SEPT) Status

SEPT Monthly Technical Progress Report
December 2001

4.1. *Summary of Status*

1. SEPT Telescope – Continued implementing the changes resulting from SEPT Team Meeting in November.
2. Sensor and E-Box Housing – Continued updating the mechanical drawings. Finished design of test mount to hold the magnets, which were delivered in November.

4.2. *Major Accomplishments*

1. Started preparations to test first magnet system, finished design of test mount for magnets and started machining in workshop.
2. Supported and participated in IMPACT Team Meeting on 14-DEC-01 at UCB.
3. Continued discussion on op-heaters and non-op heaters. Decision: place heaters and heater controls on outside surface of E-Box.
4. Temperature coefficients for the magnet material NdFeB provided to UCB and Mario Acuna.
5. Planned activities for January 2002 are:
    - finish machining magnet housing, prepare clean room for arrival of first detector stack expected for end of January, continue updating mechanical drawings for detector housing and E-Box housing.
    - Continue discussion on op-heaters and non-op heaters and in particular harness: there is a lack of redundancy in 25-pin connector and bias line between SEPT and SEP.

4.3. *Design Updates*

1. None

4.4. *Outstanding Problems*

1. No progress with respect to magnet material. Mario Acuna prefers Cerium Cobalt, our baseline is still Neodymium Iron Boron. Kiel is awaiting comments on information supplied to Mario Acuna and Chris Russell (temperature coefficients).

4.5. *New Problems*

1. Lack of redundancy in harness (25-pin MDM and coax SSMC) between SEPT and SEP due to accommodation problems for 31-pin MDM, possibly including TSQ (twisted shielded quad) wires for bias (see discussion with Branislav).

4.6. *Top Risks*

4.7. *Problem/Failure Quick Look*

5. Caltech/JPL (SEP) Status

December 2001

5.1. *Summary of Status*

Activities centered on developing a new schedule and budget, the VLSI design, detector development, and the SEP Software and GSE Software Development Plans.

5.2. *Major Accomplishments*

Schedule:

- Released the new budget/schedule in mid-December. This Project 2000 file is LET.SEP.BCDE.12.14.01.mpp. It reflects the slipped launch date to December 2005 and includes Phase E. We are now planning to deliver to JHU/APL directly (instead of UCB) on 9/1/2004 with 10.2 weeks of contingency in the schedule (i.e., we plan to be ready to deliver on 6/22/04).

Electronics:

- VLSI layout continued. Analog sections received earlier from Dean Aalami continued to be edited/integrated by Rick. Analog core is near completion. Next steps are integration of digital core elements, integration of completed core within pad frame, and final checks. Checks to include layout versus schematic and "direct from layout" simulation of digital sections (as done prior to recently successful HEFT flight chip submission).
- Continued procurement of long lead-time items for VLSI hybrid and made another revision of the hybrid's component layout diagram.
- Received quote update for EEPROM 128k x 8, 3.3V from Maxwell Technologies (formerly SEI). Project parts specialist (Antonio Reyes) reviewed the quote as well as the screening flows and made recommendations for compliance with the Grade 2 requirement. Same procedure is being done for SRAM 128k x 8, 3.3V.
- Sent manufacturers' radiation test reports on EEPROM and SRAM to the Project parts specialist for review by the radiation group at GSFC.
- Continued work on the SEP electrical ICD and the VLSI hybrid screening spec.
- Updated SEP resources table based on December team meeting presentations. There are no significant changes in mass and power.

GSE:

- Finished the IDL time conversion routines for the GSE and Detector Development system.
- Partially completed the stage movement software for the Detector Development system.

Software:

- Completed final version of LET-SEP Central Software Development Plan for team approval.

Detectors:

- First tests were completed using the L1 mask to etch thin sections on silicon wafers for L1 detectors. The resulting surface quality (smoothness) of thinned areas is poorer than achieved with some previous test etches. Samples will be sent to Micron Semiconductor to determine whether they think surface quality is good enough for detector production. Additional test etches are planned with some modifications to the process being used for the final smoothing.
- Design of the L2 detector mask was modified prior to fabrication in order to reduce the inactive border around the detector. H1 and H3 masks were modified to make the overall chip shapes be regular polygons of 16 rather than 8 sides to better conform to the shape of the circular active area. Masks designs for H2/L2 and H1/L3 were accepted once these changes had been made.
- Checkout of the vacuum system to be used for alpha-particle testing of L1 detectors at JPL continued, with several leaks being identified and corrected.

5.3. *Design Updates*

- Mass and power update sent separately.

5.4. *Outstanding Problems*

None.

5.5. *New Problems*

None.

5.6. *Top Risks.*

- Small increments of funding covering short time periods threatens our development schedule. We are constantly having to stop and re-start work at JPL. Currently the critical work on the hybrid and detector development is occurring at JPL and we are short of funds to support the activities. We need larger amounts of funding covering longer time periods (6 months or more).
- Schedule slack that we show explicitly will be taken away from us
- Development of the L1 detector. (See September report for details.) Risk mitigated by creating slack in schedule and by starting a parallel development effort using different and more conventional manufacturing technique.
- Development of the VLSI chip. (See September report for details.) Risk mitigated by providing for two more months for the layout and checking while still keeping 30 weeks for a second run if necessary.

5.7. *Problem/Failure Quick Look*

None.

6. SIT MONTHLY TECHNICAL PROGRESS REPORT

December 2001

6.1. *SUMMARY of STATUS*

a. SIT TELESCOPE -no change from last month. Prototype is in house and working.
b. SIT TOF System - Prototype TOF electronics is fully designed and is in test. Analog system arrived from MPAe.
c. SIT Energy/Logic System - Energy system design waits for more data on the Caltech PHA chip. We have begun work on possible Amptek design to replace Caltech PHA chip on SIT as a way to make progress in this area.
d. SIT HVPS - We continue to work on resolving the interconnection of the telescope and HVPS.

6.1.1. Schedule Changes

Current schedule is dated 12/4/01

6.2. *MAJOR ACCOMPLISHMENTS*

6.2.1. This Month

This month we continued testing of the digital TOF electronics on the bench and got them to work completely with the TOF GSE. We also supported the IMPACT Team Meeting and other SEP-related topics. We received the tested analog TOF electronics from MPAe. We put together a proposal for more resources to develop an Amptek alternative to the Caltech ASIC chip for use on SIT to address the schedule problem from the slippage of the ASIC delivery.

6.2.2. Next Month

We will finish bench testing the digital and analog TOF electronics and begin testing them with the prototype telescope. We will continue development of the Amptek-based energy system for SIT.

6.3. *DESIGN UPDATES*

6.3.1. Resources

	Last Month	This Month	Change
Mass (g) *	1220	1220	0
Power (mW)	1349	1349	0
Telemetry (bps)	240	418	178

* Includes 200g bookkept by GSFC for SIT structure

No changes in mass or power this month. The telemetry increased due to the increased allocation.

6.4. *OUTSTANDING PROBLEMS*

We are still not under contract and have not yet entered Phase B We need to order telescope sensor elements (solid state detectors foils and microchannel plates) in January.

6.5. *NEW PROBLEMS*

We have become concerned that the slippage of the proposed delivery of the flight Caltech ASICs and the data package necessary to design with them will impact our schedule. With the TOF testing well in hand, we need to proceed to energy system design in early 2002 and we cannot do this until we get more data from Caltech. At the recent team meeting we proposed developing an alternative energy system design for SIT based on Amptek hybrids and we outlined approximate additional resources necessary to fly such a system. We need rapid response from the project on whether to proceed with this alternative design in order to achieve maximum schedule benefit

6.6. *NEW RISKS*

Late delivery of Caltech ASICs and engineering data will impact the SIT schedule and reduce the time available for characterizing and debugging the SIT sensor. The limited manpower resources at UMd make it impossible to recover this time by rearranging the schedule.

6.6.1. Mitigation Plan

see "New Problems" above

6.6.2. Schedule

1. 1. Jan 02 - work with project to better quantify the mass, power and dollar resources needed for the plan.
2. Late Jan/Early Feb - get project approval to proceed
3. Mar 02 - Perform design of system and breadboard.
4. Late Mar 02 - provide GSFC with updated Front-End Logic requirements document so ACTEL design work can proceed.
5. Apr 02 - Board layout at UMd
6. Apr 02 - Inputs to GSFC on parts lists, thermal issues, mass and power

6.7. *PROBLEM/FAILURE QUICK LOOK*

Starts at first turn-on of flight hardware.

ID #	Description	Assignee	Opened	Closed

7. CESR (SWEA) Status

CESR- TOULOUSE- FRANCE **Author : Claude Aoustin / Project Manager**

SWEA PROGRESS REPORT # 4
(January 14, 2002)

December 2001

CESR is in charge of :
- Electrostatic analyzer with deflectors, grids and Retractable Cover
- Detector consisting of two MCP rings
- Amplifiers and discriminators
- 3 High voltages

7.1. *Summary of Status*

Mechanical design end 17/12/2001 On the way
Mechanical analyzer fabrication end 22/04/2002
Electronics fabrication end 28/01/2002 started
ETU Assembly start 06/05/2002 end 05/07/2002
Delivery to UCB 12/07/2002

7.2. *Major accomplishments*

Electrostatic analyzer design finalized. First report to be used for the thermal study sent. During the meeting hold in Berkeley on December 15, the full design was checked and discussed. Pin puller accommodation to be modified to take into account the detailed information got during this meeting.

Deflectors grids fabrication on the way.

Electronics boards are designed. Finalization of the mechanical design for the mounting of the boards done. Fabrication of the 3 electronics boards started.

7.3. *Design Updates*

Mass : 1040 g
Power : 446 mW min ; 662 mW max

7.4. *Outstanding Problems*

Pin puller : P5-403-10S
Accommodation on the way.

Thermal design :

Preliminary detailed design given to UCB and sent to Bob Eby.
Resistors added under the MCPs to heat them.

Interface with UCB section

Discussed and defined during the meeting in Berkeley 15 December.
Purging system accommodation defined too.

AMPTEKS amplifiers quality

It will difficult for us to have the best quality for them as done for Goddard

7.5. *New problems*

None

7.6. *Top Risks*

7.7. *Problem Failure Quick Look*

None

8. GSFC (MAG) Status

Nothing to report