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Subject: IMPACT Monthly Technical Progress Report, Contract NAS5-00133

Harry:

Enclosed is the monthly technical progress report for the STEREO IMPACT project for the month of November 2001.

Sincerely,

David Curtis
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CC:

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IMPACT Team

1. IMPACT Overview

This report is presented in sections by institution. Section 1 is an IMPACT Project Manager / System Engineer's overview.

1.1. *Contracting / Funding*

Subcontracts to Caltech and University of Maryland are in work (at the subcontractors). A minor glitch involving an insurance clause at Maryland is in work.

The current funding allotment has just about run out, and a new allotment is expected early December. Because of pipe-line delays in the system through to the subcontractors (Caltech and UMd) it is important that IMPACT be funded somewhat in advance of expected spending.

We expect a contract mod from Project shortly to modify the launch date. We are working on a corresponding revised budget and schedule.

We are competing our Proposal and IT Security Plan in response to the NASA RFP for "Incorporation of Security Requirements for Unclassified Information Technology Resources". This issue only impacts UCB.

1.2. *Significant System-Level Accomplishments*

- Work on PDR action item responses continues.
- November PAIP meeting resulted in some changes to the PAIP. Modifications are out for review in the team.
- Still working on parts screening issues (selecting contractors, developing details test specs), getting approvals
- Participated in EMC and Contamination Control Peer Reviews at APL
- Working operational & survival heater issues (refining thermal models)
- Reviewing several documents for sign-off at Mission PDR
- Preparing instrument presentation for Mission PDR
- Working on a number of design trades to improve reliability and meet EMC requirements.

1.3. *System Design Updates*

Mass and power spreadsheet update submitted separately (and provided to APL). No significant changes (heater requirements still open pending final results of thermal models)

1.4. *System Outstanding Issues*

- Problem with heaters – had planned external mounting, which violates EMC requirements. There will be some small mass impact in adding some kind of EMC shield.
- Non-NASA funded institutions PAIP is still not accepted by Project. We are attempting to find a compromise.

- SEP schedule is tight. Caltech is working to free up some slack. We are concerned that any slack generated may be taken away (as it recently was when delivery was pushed up a month)
- Looking at adding protection to SEP LVPS so that a failure in one instrument will not propagate into the rest.
- The current design of low voltage power distribution violates the EMC requirements (due to the break-up of STE and SEP). We are working on estimating the resource costs required to fix the system to be compliant, and at the same time, investigating if a waiver would be possible. This change goes beyond just adding extra windings to the LVPS – it affects the power distribution inside the SEP Central box, and the harness from SEP Central to the SEPT units.

1.5. *Top 10 Risks*

Top 10 risks are attached, same as last month. The project risk management database is still inaccessible.

IMPACT Top Ten Risks 11/2001

No.	Risk Item	Score	Mitigation	Mitigation Schedule						
				PDR	Bread-board Test	CDR	Sub-system Test	System Test	Env test	Early Orbit Test
UCB_5	IMPACT boom is a new design. Failure could affect Imager pointing requirements as well as boom-mounted instruments.	HIGH	Design for reliability. Early development and test to ensure reliability.	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH
UCB_21	Custom VLSI used in SEP may has schedule and cost risk	MEDIUM	Early development to prove design	MEDIUM	MEDIUM	LOW	LOW	LOW	LOW	LOW
UCB_18	LET Detectors from a new manufacturer	MEDIUM	Working with manufacturer on process	MEDIUM	MEDIUM	LOW	LOW	LOW	LOW	LOW
UCB_23	Non-standard parts qualification failure could impact delivery schedule	MEDIUM	Early parts selection and screening	MEDIUM	MEDIUM	LOW	LOW	LOW	LOW	LOW
UCB_15	GSFC Approval Requirements could delay instrument delivery or add cost	MEDIUM	Difficult to asses, history is mixed	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	LOW
UCB_4	The IDPU is a single point failure mechanisim for the IMPACT suite and	HIGH	IDPU is a simple, reliable system. Extra attention will be paid to ensuring its reliability	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH
UCB_13	IMPACT team is thin; loss of a critical	MEDIUM	Reassign work amongst team as and when required	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	LOW	LOW
UCB_11	Stringent EMI requirements may delay schedule is testing fails	MEDIUM	Careful design, early testing	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	LOW	LOW
UCB_1	ITAR restriction of information exchange with foreign CoIs may result in problems	MEDIUM	Various channels of communication have been found within the ITAR restrictions to allow adequate information flow. Some	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	LOW
UCB_2	Increasing documentation requirements distract key personnel from design tasks	MEDIUM	Negotiate documentation requirements to minimize impact	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	LOW

2. Berkeley Status

2.1. *Summary of Status*

Much of Berkeley's effort this month went into preparing for the Mission PDR and Team Meeting in December. No significant new schedule issues.

2.2. *Major Accomplishments*

SWEA/STE:

- Electronics packaging requirements provided to ME

IDPU:

- Flight Software requirements updated, and data flow charts generated
- IDPU memory map altered to increase maximum code space available to 64Kbytes
- IDPU RAM increased from 2 to 3Mbytes due to increased PLASTIC buffering requirements and to make better use of added telemetry bandwidth for burst data

LVPS/HVPS:

- Estimated resource cost for separating SEPT LVPS secondaries to meet EMC requirements.

Boom:

- Thermal model proceeding (with Eby). A simple model has been provided for the spacecraft interface. SWEA operational & survival heater requirements still pending more mechanical details of SWEA from CESR.
- Prototype boom (2 segments) ready for Mission PDR (still needs some fine-tuning).

GSE:

- IDPU Simulator hardware ready to send to UCB for integration with software.

2.3. *Design Updates*

We have repartitioned the UCB SWEA / STE-D electronics to decouple electronics lower temperature limit from detectors (which would like to be colder). This could save some heater power and simultaneously improve detector performance.

2.4. *Outstanding Problems*

- SWEA operational heater estimate needs refining based on a better thermal model. Possible modest increase in heater power requirement.

2.5. *New Problems*

None.

2.6. *Top Risks.*

No new risks identified.

2.7. *Problem/Failure Quick Look*

None.

3. GSFC (SEP) Status

STEREO/IMPACT/SEP/GSFC Progress Report for November 2001 – (von Rosenvinge, Baker, Hawk, Reames, Shuman, Wortman)

3.1. *Summary of Status*

Mostly on-schedule. The SEP ICD drawings (SEPT, SIT, LET, and HET) have now all been completed, however none has been formally incorporated into the IMPACT ICD. The L1 mount design underwent several iterations, resulting in a total schedule delay of 2 months. Completed mounts are expected in early January. The Caltech VLSI design document is incomplete, holding back analog front-end design for HET and SIT. SIT may opt to not use the Caltech VLSI chip. The delivery date for the first VLSI samples has been slipped four months but this has been offset by slipping the delivery of HET and SIT to Caltech from 6/11/03 to 12/03. Waiting on UCB for requirement changes with respect to the volume required for the Low Voltage Power Supply.

3.2. *Major Accomplishments*

- Completed ICD drawings for SEP/SEPT.
- Completed L1 detector mount design and have received bids.
- Reviewed the Contamination Control plan and made presentation at APL regarding SEP contamination control plans and requirements.
- Worked on the SEP thermal design to determine the power needed for operational and survival heaters. Still not complete.
- Completed windows-based debugger for the development of MISC assembly-language code.
- Changed the GSFC MISC design to lower the power consumption. Specifically, non-global clocking has now been implemented in the GSFC design. The power consumption of the GSFC MISC design is now essentially the same as for the Caltech design.
- Wrote a preliminary HET and SIT Software Development Plan.

3.2.1. Next Month

- Study SIT front-end logic specification (received from UofMD Oct 15).
- Complete initial SEP thermal design; this hinges on obtaining the lowest operating temperature for the Caltech VLSI chip.
- Release updated schedule.
- Work on defining HET software and hardware requirements.
- Resolve Contamination Control issue re surface cleanliness at delivery.

3.3. *Design Updates*

Currently none. Expecting the size of the Low Voltage Power Supply to increase and requirements to emerge for operational and survival heaters. In addition, it had been

expected that the survival heaters and thermostats would be applied externally by APL and that the associated weight would be charged to APL. It now appears that we are going to have to supply these ourselves and that they will need to be shielded for EMI reasons. There will be a corresponding weight penalty that has not yet been determined.

3.4. *Outstanding Problems*

We are working to adapt to the late delivery of the VLSI chips. Completion of the PHA User's Manual, detailing the operation of the Caltech VLSI chip, has been put on the Caltech schedule explicitly and is due at the end of February '02. This will assist us to be ready to hit the ground running when we do receive the VLSI chips.

3.5. *New Problems*

See preceding discussion re VLSI.

Contamination Control: In our presentation regarding contamination control, we stated our plan to deliver our instruments with the exterior surfaces cleaned to level 500 B. This is in conflict with the requirement presented by APL calling for level 300 A. This needs to be resolved.

3.6. *Top Risks*

No significant risks at GSFC?

3.7. *Problem/Failure Quick Look*

4. Kiel (SEPT) Status

SEPT Monthly Technical Progress Report
November 2001

4.1. *Summary of Status*

1. SEPT Telescope – Progress with silicon detector stack fabrication thanks to delivery of triaxial cable. However, delivery of first detector stack (expected for December 2001) is further delayed by approximately 5 weeks due to problem with light-tightness of epoxy boards. First magnet system delivered.
2. Sensor and E-Box Housing – New set of mechanical drawings finished and reviewed at SEPT Team Meeting on Nov. 5/6 at ESTEC. Some design changes were proposed to facilitate assembly and to improve stability to load and shear stresses. Resulting update of mechanical drawings in progress.
3. SEPT E-Box – Update of digital and analog board layout incorporating change requests from SEPT Team Meeting. Implementation of new grounding concept after discussion with Branislav and Dave. Decision taken on future staff assignments and contracts to outside companies to overcome manpower problem.

4.2. *Major Accomplishments*

1. First magnet system delivered. Incoming inspection performed. Magnetic properties on data sheet look good, but test with electrons from radioactive sources needed to verify proper function.
2. Detector masks ready, PIPS silicon detectors fabricated, triax cable delivered, NASA approved supplier for epoxy board FR4 (POLYCLAD) identified. Assembly into stack of two with 600 µm distance started, but problem encountered: corridor to evacuate air between the two detectors must be light-tight! Delay of about 5 weeks expected.
3. Redefinition of SEPT beacon mode data.
4. Input to IMPACT SEP Flight Software Development Plan.
5. Decision to have a full insulation: no direct DC coupling between all 3 boards (digital board, analog board, EMC shield) and the housing. Star ground inside E-Box. E-Box thermally and electrically insulated from S/C structure. Grounding via harness (optional: via strap from grounding stud).
6. Final review of digital board layout. Everything ready for population of digital board.
7. Discussion on op-heaters and non-op heaters.
8. Manpower deployment at ESTEC: new electronics engineer with 50 % of his time, starting January 2002. But: Peter will phase out as Technical Manager, candidate for this position identified but not yet approved. New software engineer for EGSE in 2002.
9. Manpower deployment in Kiel: open position for physicist announced to support assembly and calibration of the sensor. 13 applicants, final decision in January 2002, start of work in March 2002.
10. SEPT schedule streamlined with SEP milestones from Alan Cummings.
11. Planned activities for December are:

- IMPACT Team Meeting at UCB
- workshop starts machining magnet housing, detector housing, E-Box housing.
- Continue discussion on op-heaters and non-op heaters

4.3. *Design Updates*

1. New mechanical layout for board mounting, internal to E-Box, drawing date 5-DEC-2001.

4.4. *Outstanding Problems*

1. Progress is made with magnetic cleanliness problem: SEPT stray field will be measured with Mario's equipment at GSFC, already for ETU. New concern raised by Mario: magnetic instability of NdFeB due to drifts with temperature or handling. He prefers Cerium Cobalt. Assessment not yet finished. Will have impact on weight (lower magnetic remanence requires larger magnets), costs (all magnets already manufactured), and schedule (new telescope design due to geometry changes).

4.5. *New Problems*

1. We have no provisions made for op-heaters and non-op-heaters inside of E-Box. Redesign would have major impact on weight (extra 130 g), costs (new board layout for thermostats, routing, EMI shielding, connector pin-out), and schedule. Our experience with Ulysses, SOHO, and Chandra is: apply heaters on outside surface, done by S/C contractor after delivery and acceptance test of flight units!

4.6. *Top Risks*

4.7. *Problem/Failure Quick Look*

5. Caltech/JPL (SEP) Status

November 2001

5.1. *Summary of Status*

Activities centered on developing a new schedule and budget, the VLSI design, detector development, and the SEP Software and GSE Software Development Plans.

5.2. *Major Accomplishments*

Schedule:

- Worked on a new budget/schedule to reflect the slipped launch date and to include Phase E. Also we have to accommodate a new delivery date to UCB, which is 6 weeks earlier than planned (now Aug 10, 2004). We created significant slack in the schedule. For more details, see October 2001 report. The new budget/schedule will be released in early December.

Electronics:

- PHA chip layout: All modules are now in the hands of Rick Cook who is assembling and editing them. We are still on track for a January submission date.
- We have agreed on a clean method for synchronizing the 1-minute data accumulation intervals and that data will be transferred from the instruments to the SEP DPU in complete packets. Instrument data rate allocations will be slightly modified to obtain integral numbers of packets per minute from each instrument. Details will be forthcoming in instrument-SEP DPU ICDs. (We await word about a possible 50% increase in t/m rate.)
- Submitted SEP Power Flow diagram to the LVPS designer at UCB (Peter Berg).
- Clarified survival and operational heater harness requirements and are now making modifications to the intra-SEP harness and connectors.
- Continued review of long lead-time parts' quotes and screening flows with help from Project parts specialist (Antonio Reyes).
- Upgraded to P-CAD 2001 PCB layout software to be compatible with subcontractor (Space Instruments); working on installing a better auto-router for Protel 99, the in-house PCB layout software.
- Flight VLSI hybrid packages arrived from NTK as promised.
- Started writing the VLSI hybrid screening spec.
- Resources update: no change, there will be change next month due to harness and connector update.

GSE:

- Revised GSE Software Development Plan.
- Continued the initial design of the GSE display software.
- Began writing IDL time conversion for GSE and Detector Development System.
- Began the design of stage movement software for Detector Development System.
- Wrote IDL software for decoding compressed spectra.

Software:

- Work continued on the SEP Flight Software Development Plan.

Detectors:

- Fabrication of the mask set for the L1 detectors was completed. The masks that are to be used for the silicon wafer thinning were shipped to Berkeley where the thinning will be done by JPL personnel.
- Initial oxidations of the front surfaces of the silicon wafers to be used for L1 fabrication were done at Micron Semiconductor in preparation for the patterning of the junction surface of the detectors.
- Fabrication of masks for the H1, H3, L2, and L3 detectors was approved, pending a change in the shape of the overall chip from octagonal to 16-sided to better approximate a circle.
- Vibration test of 3 "pre-prototype" L1 detectors was done with no failures.
- Backup L1 option is being pursued in case problems are encountered with baseline approach. Micron will make prototype L1 using "conventional" approach starting from lapped and polished 20 μ-thick silicon wafers

5.3. *Design Updates*

No mass and power changes.

5.4. *Outstanding Problems*

None.

5.5. *New Problems*

None.

5.6. *Top Risks*

- Schedule slack that we show explicitly will be taken away from us. We recently lost 2 weeks in the development schedule because it was showing that we could deliver to UCB on 9/10/04, when the agreement was 9/24/04. UCB interpreted the schedule as reflecting a 9/10/04 delivery date. Then word was spread that we had 30 weeks of slack in certain parts of our schedule. Shortly thereafter we had our delivery date moved back a month.
- Development of the L1 detector. (See September report for details.) Risk mitigated by creating slack in schedule and by starting a parallel development effort using different and more conventional manufacturing technique.
- Development of the VLSI chip. (See September report for details.) Risk mitigated by providing for two more months for the layout and checking while still keeping 30 weeks for a second run if necessary.

5.7. *Problem/Failure Quick Look*

None.

6. SIT MONTHLY TECHNICAL PROGRESS REPORT

6.1. *SUMMARY of STATUS*

a) SIT TELESCOPE - ICD produced at GSFC. Ceramic parts received. Some others ready to go out.
b) SIT TOF System - Prototype TOF electronics is fully designed and is in test. The digital system is at UMd for testing on the bench and with the prototype telescope. The analog system is at MPAe for bench and thermal vacuum testing.
c) SIT Energy/Logic System - Front end logic design requirements have been specified. Work on this is continuing at GSFC. Energy system design waits for more data on the Caltech PHA chip.
d) SIT HVPS - We continue to work on resolving the interconnection of the telescope and HVPS.

6.1.1. Schedule Changes

Moved receipt of flight Caltech PHA chips from 4/18/02 to 6/18/02 per list of milestones from Alan Cummings 11/20/01. This uses up the slack we had between the delivery of these units and the need date to install them in the SIT SN1 energy board. Current schedule is dated 12/4/01

6.2. *MAJOR ACCOMPLISHMENTS*

6.2.1. This Month

This month we began testing of the digital TOF electronics on the bench. We also supported the PAIP review and provided inputs to the contamination control plan, beacon telemetry and other IMPACT and SEP issues. We began work on the SIT SW Requirements document. At MPAe the digital TOF electronics were successfully tested with the analog system. The prototype analog TOF electronics were successfully put through a thermal vacuum test.

6.2.2. Next Month

We will continue testing the digital TOF electronics with the prototype telescope. We also expect to receive the revised prototype analog TOF electronics from MPAe and to begin testing of the entire TOF system. We will also support the IMPACT team meeting.

6.3. *DESIGN UPDATES*

6.3.1. Resources

	Last Month	This Month	Change
Mass (g) *	1220	1220	0
Power (mW)	1349	1349	0
Telemetry (bps)	240	240	0

* Includes 200g bookkept by GSFC for SIT structure

No changes in mass power or telemetry this month. We have increased the beacon mode data to 3.2 bits/sec..

6.4. *OUTSTANDING PROBLEMS*

We are still not under contract and have not yet entered Phase B We need to order telescope sensor elements (solid state detectors foils and microchannel plates) in January.

6.5. *NEW PROBLEMS*

Concern about PHA chip schedule.

6.6. *NEW RISKS*

None

6.6.1. Mitigation Plan

6.6.2. Schedule

6.7. *PROBLEM/FAILURE QUICK LOOK*

Starts at first turn-on of flight hardware.

ID #	Description	Assignee	Opened	Closed

7. CESR (SWEA) Status

CESR- TOULOUSE- FRANCE **Author : Claude Aoustin / Project Manager**

SWEA PROGRESS REPORT # 2
(December 11, 2001)

November 2001

CESR is in charge of:
- Electrostatic analyzer with deflectors, grids and Retractable Cover
- Detector consisting of two MCP rings
- Amplifiers and discriminators
- 3 High voltages

7.1. *Summary of Status*

Mechanical design end 17/12/2001 On the way
Mechanical analyzer fabrication end 22/04/2002
Electronics fabrication end 28/01/2002 started
ETU Assembly start 06/05/2002 end 05/07/2002
Delivery to UCB 12/07/2002

7.2. *Major accomplishments*

Electrostatic analyzer design finalized. First report to be used for the thermal study sent. Deflectors grids fabrication on the way.

Electronics boards are designed. Finalization of the mechanical design for the mounting of the boards done. Fabrication of the 3 electronics boards started.

7.3. *Design Updates*

Mass : 1040 g NEW !
Power : 446 mW min ; 662 mW max

7.4. *Outstanding Problems*

Pin puller : P5-403-10S
We got all the necessary information from Michael Bokaie (tiniaerospace) with the help of Paul Turin (SSL). It has been integrated into the design.

Thermal design :
Preliminary study is showing that the temperature will be too low for the power on. Full study should be necessary to freeze the design. The results will have impact on the interface attachment point between the different items. Preliminary detailed design sent to Bob Eby.

URGENT : Interface with UCB section
Has to be defined clearly : mechanical, electrical connection (routing cables) and purging system location. We will discuss these points during the SWEA splinter meeting in Berkeley on December 15. We have routed the tube for the purging through our electronics boards.

AMPTEKS amplifiers quality
It will difficult for us to have the best quality for them as done for Goddard

7.5. *New problems*

None

7.6. *Top Risks*

7.7. *Problem Failure Quick Look*

None

8. GSFC (MAG) Status

Nothing to report