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Subject: IMPACT Monthly Technical Progress Report, Contract NAS5-00133

Harry:

Enclosed is the monthly technical progress report for the STEREO IMPACT project for the month of October 2001.

Sincerely,

David Curtis
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CC:

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IMPACT Team

1. IMPACT Overview

This report is presented in sections by institution. Section 1 is an IMPACT Project Manager / System Engineer's overview.

1.1. *Contracting / Funding*

Subcontracts to Caltech and University of Maryland are in work (at the subcontractors).

UCB expects the current funding allotment to run out in late November or early December. Because of pipe-line delays in the system through to the subcontractors (Caltech and UMd) it is important that IMPACT be funded somewhat in advance of expected spending.

We expect a contract mod from Project shortly to modify the launch date. We are working on a corresponding revised budget and schedule.

1.2. *Major System-Level Accomplishments*

- Work on PDR action item responses continues.
- Completed UCB GSE Software Development Plan submitted.
- Work on the spacecraft ICD continues.
- Working on a number of design trades to improve reliability and meet EMC requirements.
- A new draft of the IMPACT IDPU/Instrument ICD has been released.
- A new version of the IMPACT PAIP has been submitted along with responses to GSFC comments on previous version in preparation for a meeting in November.
- An updated boom suite schedule has been published
- More parts screening houses have provided quotes; some are somewhat lower than previous bids.

1.3. *System Design Updates*

Mass and power spreadsheet update submitted separately (and provided to APL). No significant changes.

1.4. *System Outstanding Issues*

- Looking at adding protection to SEP LVPS so that a failure in one instrument will not propagate into the rest.
- The current design of low voltage power distribution violates the EMC requirements (due to the break-up of STE and SEP). We are working on estimating the resource costs required to fix the system to be compliant, and at the same time, investigating if a waiver would be possible. This change goes beyond just adding extra windings to the LVPS – it affects the power distribution inside the SEP Central box, and the harness from SEP Central to the SEPT units.

1.5. *Top 10 Risks*

Top 10 risks are attached, re-ordered by risk. Note that risk UCB_16 has been downgraded off the top 10 list – prototype detectors meet requirements. The project risk management database is still inaccessible.

IMPACT Top Ten Risks 10/2001

No.	Risk Item	Score	Mitigation	Mitigation Schedule						
				PDR	Bread-board Test	CDR	Sub-system Test	System Test	Env test	Early Orbit Test
UCB_5	IMPACT boom is a new design. Failure could affect Imager pointing requirements as well as boom-mounted instruments.	HIGH	Design for reliability. Early development and test to ensure reliability.	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH
UCB_21	Custom VLSI used in SEP may has schedule and cost risk	MEDIUM	Early development to prove design	MEDIUM	MEDIUM	LOW	LOW	LOW	LOW	LOW
UCB_18	LET Detectors from a new manufacturer	MEDIUM	Working with manufacturer on process	MEDIUM	MEDIUM	LOW	LOW	LOW	LOW	LOW
UCB_23	Non-standard parts qualification failure could impact delivery schedule	MEDIUM	Early parts selection and screening	MEDIUM	MEDIUM	LOW	LOW	LOW	LOW	LOW
UCB_15	GSFC Approval Requirements could delay instrument delivery or add cost	MEDIUM	Difficult to asses, history is mixed	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	LOW
UCB_4	The IDPU is a single point failure mechanisim for the IMPACT suite and	HIGH	IDPU is a simple, reliable system. Extra attention will be paid to ensuring its reliability	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH
UCB_13	IMPACT team is thin; loss of a critical	MEDIUM	Reassign work amongst team as and when required	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	LOW	LOW
UCB_11	Stringent EMI requirements may delay schedule is testing fails	MEDIUM	Careful design, early testing	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	LOW	LOW
UCB_1	ITAR restriction of information exchange with foreign CoIs may result in problems	MEDIUM	Various channels of communication have been found within the ITAR restrictions to allow adequate information flow. Some	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	LOW
UCB_2	Increasing documentation requirements distract key personnel from design tasks	MEDIUM	Negotiate documentation requirements to minimize impact	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	LOW

2. Berkeley Status

2.1. *Summary of Status*

A new IMPACT boom suite schedule has been published. The boom prototype schedule remains challenging (delivery of a multi-joint prototype by S/C PDR).

2.2. *Major Accomplishments*

SWEA/STE:

- The STE preamp noise meets the requirements, but there is room for improvement. The problem has been isolated in the FET. A test with a colder FET is required to see if we want to separate the FET from the rest of the preamp and run it colder. Some issues with detector bonding need to be worked with LBNL.
- A breadboard of the SWEA/STE interface is partially built; testing to be started next month. A form factor has been decided on and layout is expected to start in about 1 month (after breadboard testing completes). Design has been modified to eliminate one non-standard part type.
- Preliminary STE cover actuator design complete. Work on preamp packaging and sunlight collimator in progress.

IDPU:

- The serial interface specification has been updated to change sample time code (h:m:s format rather than binary seconds)
- PWB form factors are being iterated

LVPS/HVPS:

- LVPS breadboard delayed due to parts issues and requirements changes. Hope to get breadboard completed next month.
- SWEA LVPS form factors for IDPU & SWEA decided.
- SIT HVPS HV connection details in work with UMd.

Boom:

- Thermal model proceeding (with Eby). Effort concentrated on providing a model for the spacecraft interface. SWEA operational & survival heater requirements still pending more mechanical details of SWEA from CESR.
- Looking at possibility of meeting Mario's desire to get the MAG into sunlight to minimize MAG heater requirements. To generate a candidate ICD drawing change to APL/Mario next month.
- Working on piece-part drawings for ETU (2 or 3 segment) boom planned for completion by Spacecraft PDR.

GSE:

- First IDPU Simulator GSE hardware has been built. Debug of circuit, FPGA, and software in progress. First delivery to UCB is expected in November/December.
- The interface driver for the host PC is completed and being worked into the user interface.

2.3. *Design Updates*

No changes.

2.4. *Outstanding Problems*

- SWEA operational heater estimate needs refining based on a better thermal model. Possible modest increase in heater power requirement.

2.5. *New Problems*

None.

2.6. *Top Risks.*

No new risks identified.

2.7. *Problem/Failure Quick Look*

None.

3. GSFC (SEP) Status

STEREO/IMPACT/SEP/GSFC Progress Report for October, 2001 - (von Rosenvinge, Baker, Hawk, Reames, Shuman, Wortman)

3.1. *Summary of Status*

Mostly on-schedule. Behind schedule re SEPT ICD drawings (will be submitted on November 14). L1 mount design underwent several iterations resulting in a schedule delay of about one month. VLSI design document is incomplete, holding back analog front-end design for HET and SIT. The delivery date for the first VLSI samples has been slipped four months but this is offset by slipping the delivery of HET and SIT to Caltech from 6/11/03 to 12/9/03. Waiting on UCB for requirement changes with respect to the volume required for the Low Voltage Power Supply.

3.2. *Major Accomplishments*

Completed ICD drawings for SEP/SIT, LET, HET.

Worked on L1 detector mount design.

Have responded to all but two RFAs from the SEP PDR. Work on the SEP thermal design has been on-going to address one of these (RFA 28). Detailed analysis of the SEPT magnetic stray-field has been completed and just needs to be summarized to complete the response to RFA 13.

Have largely verified the GSFC MISC design. One change was made to the design in order to bring it into compliance with an unadvertised feature of the Caltech MISC design.

Developed debug monitor code for MISC.

Next Month-

Complete replies to last two PDR action items (RFAs 13 and 28).

Review the Contamination Control plan; make presentation for meeting at APL regarding SEP contamination control plans and requirements.

Study SIT front-end logic specification (received from UofMD Oct 15).

Complete L1 mount design and put out for fabrication.

Complete initial SEP thermal design.

Complete SEP Software Development Plan.

Release updated schedule.

Complete windows-based debugger for the development of MISC assembly-language code.

Investigate changes to the GSFC MISC design to lower the power required. Specifically, the Caltech design includes non-global clocking which has yet to be implemented in the GSFC design.

3.3. *Design Updates*

Currently none. Expecting the size of the Low Voltage Power Supply to increase and requirements to emerge for operational and survival heaters.

3.4. *Outstanding Problems*

No major problems. Late involvement of analog engineer due to not having the necessary VLSI specifications could be a problem.

3.4.1. New Problems

The delivery date of initial VLSI from Caltech has been slipped by 4 months. The delivery dates of SIT and HET to Caltech have been slipped ~6 months in order to ameliorate this. It was realized that the original delivery dates were based on a single central processor for SEP; the new design with separate MISCs in SIT, LET, and HET requires significantly less integration and test time at Caltech, making it possible for Caltech to receive SIT and HET later.

3.5. *Top Risks*

No significant risks at GSFC?

3.6. *Problem/Failure Quick Look*

4. Kiel (SEPT) Status

Date:	13-Nov-01
Period covered:	October 2001
Activity covered:	SEPT instrument development
Institution:	University of Kiel, ESTEC
Compiled by:	R. Mueller-Mellin, P. Falkner

4.1. *Summary of Status*

The model calculation of the far field with mismatched magnetic dipoles has been initiated. Delivery of magnet systems is postponed to await conclusions. The Electronics-box design has been completed in Kiel and awaits concurrence by ESTEC, expected during SEPT Team Meeting scheduled for Nov. 5/6. The sensor design has been completed, but mechanical drawings must still be updated to reflect minor design details. The detector stack fabrication was stopped for two weeks to incorporate the recent sensor design changes and has been resumed afterwards. The triax cable which was ordered in September is still not delivered due to Dutch distributor who requests advance payment, but money orders between Germany and the Netherlands take time. This delays fabrication of the first detector stack at Canberra, delivery now expected for December 2001. The first programmed prototype FPGA is delivered to ESTEC on Oct. 1. Analog board (breadboard model) is ready for test, but PDFE ASICs not yet mounted. Analog board test bench is finished. Digital board is ready for test. Digital board test bench is not yet ready.

4.2. *Major Accomplishments*

1. Hi-Rel components for FPGA 54SX32S ordered for SEPT.
2. Board assembly into housing (sandwich construction) updated.
3. Decision to have a full insulation (no direct DC coupling) between all 3 boards and the housing.
   The Ground contact will be done via a cable connection to the box grounding stud.
4. Two contracts – one for FPGA EM and FM development and verification, one for electrical testing and debugging of SEPT electronics have been raised to overcome the manpower problem at ESTEC.
5. Management meeting at ESTEC to improve manpower situation scheduled for 9-Nov-2001. Expected results: Additional manpower to be provided (internal and external), but might take some time for full deployment (contract issues!) .
6. Update of SEPT electronics power supply requirements.
7. Update of SEPT electronics mass break down.
8. The Far Field Analysis was completed and circulated, positive answer received from Mario Acuna (he tolerates 1.33 nT, (matched case) but not 4.00 nT (mismatched case). The latter can be avoided by high precision measurements of the remanence of the individual magnets and careful selection of the four magnets constituting the deflection system.
9. Input to thermal analysis was prepared and sent to John Hawk, GSFC thermal engineer.
10. Draft schedule in Project 2000 format established.

11. EGSE: the PC hardware is assembled, the programming is still open, but paperwork is in progress to select a contractor.

Planned activities for November are:

- SEPT Team Meeting at ESTEC reviewing mechanical and electrical design
- updating mechanical interface control drawings to reflect results of review
- updating circuit diagram and board layout to reflect results of review
- updating power and mass breakdown after incorporation of updates
- incoming inspection for the magnet system.
- streamline SEPT draft schedule with SEP milestones from Alan.

4.3. *Design Updates*

1. 25 pin MDM connector CBR type, 90 ° PCB mounted . Gender changed to socket (as requested by Branislav).
2. There are some new restriction for placement of components on the PCB: the interboard connectors need to be at least 1 mm away from PCB border. Place of the MDM connector has to be fixed (distance from box walls, precise location on digital board).
3. Begin of Revision 1.0 schematics design.

4.4. *Outstanding Problems*

1. Progress is made with magnetic cleanliness problem. PDR RFA #13 is considered closed from SEPT side. How to verify the stray field at a distance of 3 to 4 meters is still open. No such measurement equipment exists in Kiel.
2. Stray light problem (PDR RFA #29) continues to exist until solar simulation test is baselined.
3. Grounding scheme for SEPT was further clarified. Final solution is still pending.

4.5. *New Problems*

4.6. *Top Risks*

4.7. *Problem/Failure Quick Look*

5. Caltech/JPL (SEP) Status

October 2001

5.1. *Summary of Status*

Activities centered on the VLSI design, the MISC development, detector and parts procurements, and the SEP Software and GSE Software Development Plans. In preparation for the modification to the Contract that is coming, a new schedule and budget was started. With the new plan of having separate MISCs in SIT, LET, and HET, it was realized that the integration and test portion of the schedule could be compressed (from 15 months to 12 months). In addition, it was realized that it was important to get SEPT delivered first because the SEP Central MISC will need to run it. The other sensors are much more independent and SEP Central does not even reformat the data. Another advantage to integrating SEPT first is that it does not use the Caltech VLSI. Thus the tight schedule we had for the VLSI has been loosened so that now we plan to do more thorough checking before submission, delay submission by 2 months, and still have 30 weeks of total slack in the schedule. By having SEPT arrive first (and yet two weeks later than originally planned) and compressing the I&T schedule we were able to move the need date for HET 5.5 months later. By having LET deliver later, more slack was also created in the L1 detector schedule (now = 30 weeks). Thus schedule slack has been created in our two biggest risk items: the VLSI and L1. The schedule is still being worked and will be released in November.

5.2. *Major Accomplishments*

Contract:

- The Contract was received and a proposal corresponding to the contract is being prepared for Caltech's Sponsored Research.

Design reviews:

- Worked on RFAs from the PDR.

Electronics:

- PHA chip layout: most modules layout complete, checking of modules (layout versus schematic) in progress. Rick: preamp layout completed, check in progress. Dean: analog backend amplifier sections layout and check complete, working on integration of the backend sections. Jill: most of digital sections layout and check complete, continuing on remaining digital sections.
- MISC developments: More experience accumulated with MISC in ACTELs. ACTEL with complete MISC + logic system designed, routed, programmed, and tested for balloon payload -- demonstrating that comparable systems for STEREO should pose no unanticipated problems. Some ACTELs with MISCs programmed for Dr. Ting's use in Chinese E-book project. (We get a lot of free exercise of our MISC design, feedback of any problems, etc., and maintain contact with Dr. Ting.) ACTEL programming software updated to improve 54sx72a programming yield, which had been only 70%.
- Agreement reached to raise the baud rate on the serial interfaces between the central MISC and the LET, HET, SIT, and SEPT from 9600 baud to 57,600 baud, allowing

faster serial boot and providing enough bandwidth to eliminate the need for any extra data links during accelerator testing.

- Agreement reached to not include a 1553 interface to the S/C in SEP, but rather stick with the original plan of interfacing through the IMPACT DPU.
- We continued evaluation of design options in response to PDR action items for SEPT isolation and LVPS short-circuit protection. Response from SEPT team and GSFC/JPL parts specialists will help resolve the open issues.
- VLSI hybrid parts procurement started with ordering of the long-lead items such as ceramic packages from NTK and chip resistor arrays from Mini-Systems.

GSE:

- Work continued on the GSE Software Development Plan in preparation for a meeting with the Project office on 6 November.
- Initial design of the display software begun.

Software:

- Work continued on the SEP Flight Software Development Plan in preparation for a meeting with the Project office on 6 November.
- Began work on the "Fast Sort" algorithm for LET event processing.

Detectors:

- Design of mask set for L1 detectors was approved and sent out for fabrication at the end of October.
- Silicon wafers for L1 fabrication were purchased by Micron Semiconductor. A few were sent to JPL to be used for checking the detector thinning process. The rest were started through production at Micron.
- Minor modifications of mask designs for the H1, H3, L2, L3 detectors were completed at Micron in response to comments from the HET/LET team. After a final review those should be approved for fabrication in November.
- The HET/LET team is interested in pursuing a parallel effort to develop L1 detectors manufactured using conventional processing starting from lapped and polished thin wafers. A formal quotation for this effort will be obtained from Micron Semiconductor in November. If it is close to the verbal estimate already obtained from Micron ($30k), a purchase order will be placed to get this effort underway. This effort addresses one of the top risks to the LET development.

5.3. *Design Updates*

No mass and power changes since last report.

5.4. *Outstanding Problems*

None.

5.5. *New Problems*

None.

5.6. *Top Risks*

- Development of the L1 detector. (See last month's report for details.) Risk mitigated by creating slack in schedule and by starting a parallel development effort using different and more conventional manufacturing technique.

- Development of the VLSI chip. (See last month's report for details.) Risk mitigated by providing for two more months for the layout and checking while still keeping 30 weeks for a second run if necessary.

5.7. *Problem/Failure Quick Look*

None.

6. SIT MONTHLY TECHNICAL PROGRESS REPORT
October 2001

6.1. *SUMMARY of STATUS*

a. SIT TELESCOPE - Existing design parts quoted and ready to be ordered. Internal HV bias connection pins identified.

b. SIT TOF System - The digital portion of the TOF electronics is in house along with the design document specifying interface requirements.

c. SIT Energy/Logic System - Front end logic design requirements have been specified. Work on this is continuing at GSFC.

d. SIT HVPS - We are working to resolve the issue of where to locate the HV divider - at the HVPS or in the telescope. Putting the divider into the telescope cuts the number of wires between the HVPS and the telescope but will force a redesign of at least some of the components of the existing telescope.

6.1.1. Schedule Changes
None. Our current schedule is dated 8/20/01

6.2. *MAJOR ACCOMPLISHMENTS*

6.2.1. This Month
This month we generated the front-end logic design requirements and supplied them to GSFC. We also answered RFAs from the previous month's PDR
A detailed Digital TOF interface document was received from TUB followed a week later by the prototype TOF electronics. We began working to integrate the new document into our existing test setup with the goal of testing the digital TOF next month.
Work on the contract with UCB continued, approving the Statement of Work and working on an updated budget.

6.2.2. Next Month
We expect to test the digital TOF next month.

6.3. *DESIGN UPDATES*

6.3.1. Resources

	Last Month	This Month	Change
Mass (g) *	1220	1220	0
Power (mW)	1340	1349	9
Telemetry (bps)	240	240	0

* Includes 200g bookkept by GSFC for SIT structure

Discussion: The power increase is from the increasing the common LVPS voltages from +/-12 to +/-13. The increase is largely due to fixed currents in several circuits that dissipate more power at higher voltage.

6.4. *OUTSTANDING PROBLEMS*

We are still not under contract and have not yet entered Phase B

6.5. *NEW PROBLEMS*

None

6.6. *NEW RISKS*

None

6.6.1. Mitigation Plan

6.6.2. Schedule

6.7. *PROBLEM/FAILURE QUICK LOOK*

Starts at first turn-on of flight hardware.

ID #	Description	Assignee	Opened	Closed

7. CESR (SWEA) Status

CESR- TOULOUSE- FRANCE **Author : Claude Aoustin / Project Manager**

SWEA PROGRESS REPORT # 2
(November 13, 2001)

October 2001

CESR is in charge of :
- Electrostatic analyzer with deflectors, grids and Retractable Cover
- Detector consisting of two MCP rings
- Amplifiers and discriminators
- 3 High voltages

7.1. *Summary of Status*

Mechanical design end 17/12/2001 On the way
Mechanical analyzer fabrication end 22/04/2002
Electronics fabrication end 28/01/2002 will start soon
ETU Assembly start 06/05/2002 end 05/07/2002
Delivery to UCB 12/07/2002

7.2. *Major accomplishments*

Electrostatic analyzer design under finalization. Last verification of the design (starting from the schematics) has been done using simulation software. Schematics and information have been given to the subcontractor. Detailed preparation of the fabrication on the way. First report to be used for the thermal study will be ready soon. Final report by the end of November for verification. Fabrication will start at the beginning of next year. Deflectors grids fabrication will start soon.

Electronics boards are designed. Finalization of the mechanical design for the mounting of the boards done. Fabrication of the 3 electronics boards will start soon.

7.3. *Design Updates*

Mass : 1210 g
Power : 446 mW min ; 662 mW max
No change from PDR

7.4. *Outstanding Problems*

URGENT :Pin puller : P5-403-10
More information are needed to be able to implement it on the top of the analyzer. The best should be to get a sample to determine precisely the interface. This is stopping the finalization of the mechanical design

Thermal design :
Preliminary study is showing that the temperature will be to low for the power on. Full study should be necessary to freeze the design. The results will have impact on the interface attachment point between the different items. We will send as soon as possible (probably mid November) the preliminary detailed design to Bob Eby.

URGENT : Interface with UCB section
Has to be defined clearly : mechanical, electrical connection (routing cables) and purging system location. This is stopping the finalization of the mechanical design.

AMPTEKS amplifiers quality
It will difficult for us to have the best quality for them as done for Goddard

7.5. *New problems*

None

7.6. *Top Risks*

7.7. *Problem Failure Quick Look*

None

8. GSFC (MAG) Status

Nothing to report