SEPT Operation Control And Data Processing Requirements

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VERSION 1.1

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1 Objectives

The purpose of this document is to describe the foreseen operation control of the SEPT instrument by the SEP central processor. The description is based on the version 1.1 of the FPGA controlling the SEPT instrument and on foreseen modifications for the flight model. The possible modifications that may occur for the final flight version of the FPGA are described in section 6. These modifications are minor and will not change the general philosophy of the SEPT operation control.

2 Revision History

- Version 0.1 to 0.4: Sept-2002 – Preliminary drafts.
- Version 0.5: Sept 2002- First release
- Version 1.0: Oct. 2002: includes comments of R. Mueller-Mellin +
    - Spelling corrected
    - Addition of Acronyms
    - Reaction to interrupts: separate section has been made to introduce the status word.
    - Calibration mode detailed.
    - Nominal mode detailed
    - Detail on timing specifications (9.5)
    - No separation between nominal mode and beacon mode at the command level.
    - Look up table specifications updated.
    - The use of the command cClearIrq has been reviewed in the pre/post operation sequence.
    - Correction of the calibration configuration sequence (10.4)
    - Data processing requirement for nominal, calibration and test generator merged.
    - Binning indexes for the beacon mode.
- Version 1.1: Oct 2002
    - Status word extended to contain operational mode designator
    - Table 15 last row changed to >2200.
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3 Applicable Documents

AD1 SEPT - FPGA Data Sheet – Second Prototype Release Document (Version 1.1b) - June 2002, Gaisler Research.

AD2 RS-232 EIA/TIA Standard

AD3 Particle Detector Front End, Preliminary datasheet, IMEC, Nov. 28, 2000

4 Acronyms and Abbreviations

FPGA Field Programmable Gate Array
LUT Look Up Table
PDFE Particle Detector Front End
SEP Solar Energetic Particles
SEPT Solar Electron Proton Telescope
SSD Solid State Detector
TBD To be defined
TBC To be confirmed
TBA To be added

5 Overview

5.1 Introduction

SEPT consists of two identical electronic units (SEPT-NS and SEPT-E) per STEREO spacecraft dedicated to the measurements of electrons (from 20 keV to 400keV) and ions (20 keV to 7 MeV). Each electronics unit analyses the signals of four solid state detectors (SSD) and four corresponding guard rings. The four detectors are integrated in two opposite oriented telescopes, either in north-south (NS) or ecliptic (E) orientation. Each detector is connected to a PDFE (Particle Detector Front End) ASIC. Additional 9 housekeeping signals per unit are sampled and transferred to SEP-DPU as well as general status. A specific test generator permits control of the electronics in flight. The low-level operation of SEPT electronics is controlled by a specific FPGA. The high level operation of SEPT is controlled by the SEP central processor by means of commands sent on the serial interface. The same serial interface is used to transfer all scientific, calibration and housekeeping data from SEPT to SEP-DPU.
The block diagram in Figure 1 shows more details for one of the two SEPT telescope units (SEPT-NS and SEPT-E).

5.2 Block Diagram

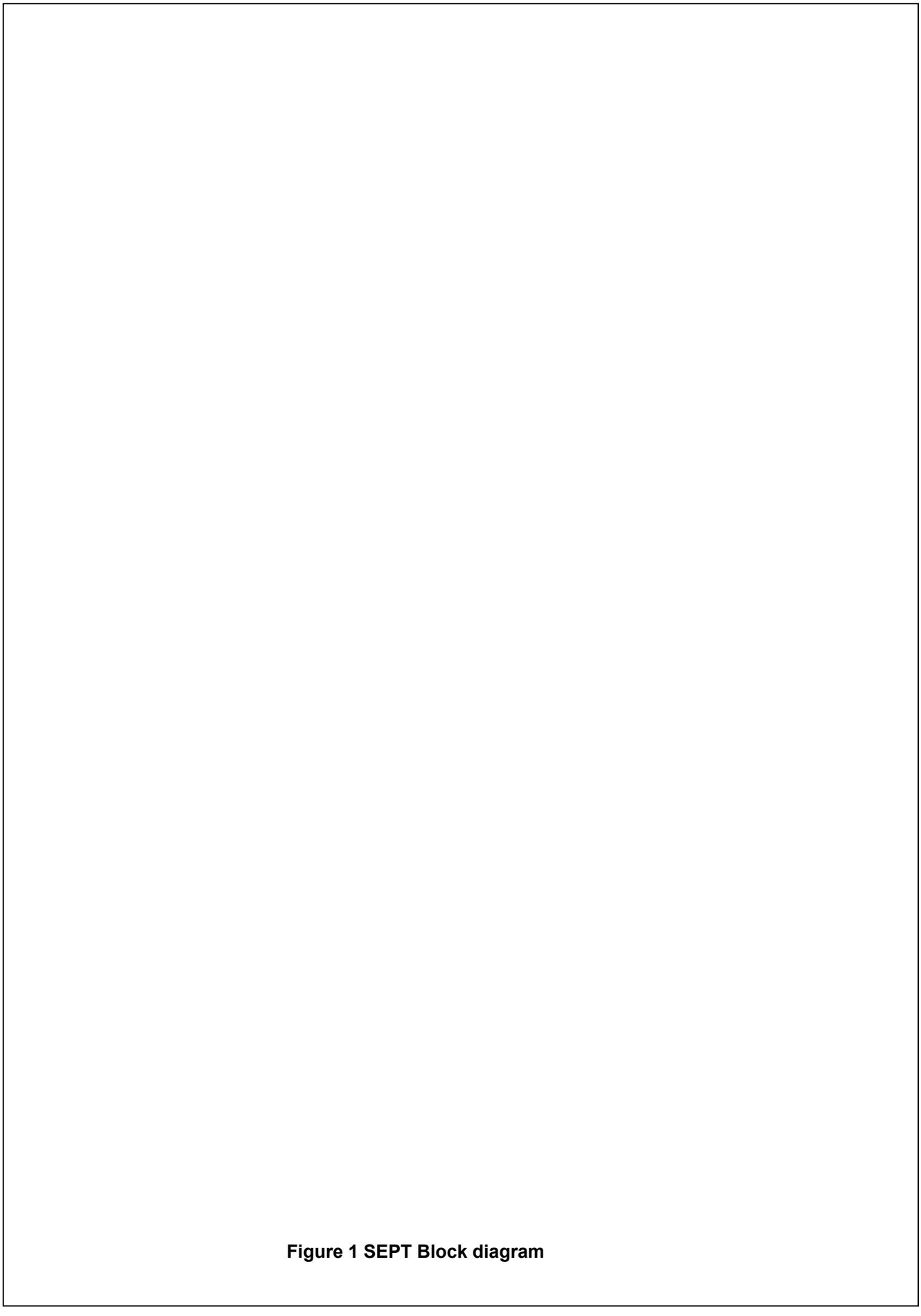

Figure 1 SEPT Block diagram

5.3 Housekeeping

The following table lists the housekeeping channels in each SEPT unit[1].

Housekeeping Variable	Description
HK_T	Temperature of the electronics
HK_CS0	Leakage current of center segment linked to PDFE0
HK_CS1	Leakage current of center segment linked to PDFE1
HK_CS2	Leakage current of center segment linked to PDFE2
HK_CS3	Leakage current of center segment linked to PDFE3
HK_GR0	Leakage current of guard ring linked to PDFE0
HK_GR1	Leakage current of guard ring linked to PDFE1
HK_GR2	Leakage current of guard ring linked to PDFE2
HK_GR3	Leakage current of guard ring linked to PDFE3

Table 1: Housekeeping channels that will be measured.

HK_T shall be used by the SEP central processor to control the operational heater.

Note: the main channel of a PDFE is connected to the central segment (CS) of one detector; the coincidence channel is connected to the corresponding guard ring (GR).

6 Expected modifications for FM

The following commands will change for the flight model and are consequently not compatible with AD1.

- cGetHK structure may change
- cConfCal structure may change
- Signification of bit 5 of the interrupt register

7 Communication specifications

7.1 Asynchronous serial link

The communication between the SEPT instrument and the SEP central processor is made through an asynchronous serial link (compliant with AD2) with the parameters shown in Table 2, and Table 3.

Setting	Value
Baud rate	57600
Start bit	1
Data bits	8
Stop bits	2

Table 2: Serial Communications settings

[1] A SEPT unit will always refer to SEPT-NS or SEPT-E

Asynchronous RS232 type format	start	D0	D1	D2	D3	D4	D5	D6	D7	Stop	Stop
	first	LSB							MSB		last
General data format i={0,n}		8*i+7	8*i+6	8*i+5	8*i+4	8*i+3	8*i+2	8*i+1	8*i		
		last							first		

Table 3 Asynchronous bit serial data format

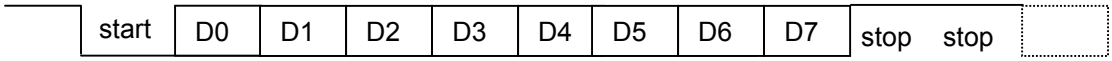

Figure 2 Serial link waveform format

No handshaking is required. Positive logic is considered for the data bits.

Some additional information is needed. The UART is built inside the SEPT FPGA. The bit rate for the transceiver is based on a 4.5 MHz internal clock (derived from the 18 MHz external clock).
The output rate is 57 692.3 baud (within 1.6% of 57600). This is derived by dividing 4.5 MHz with 78. On receipt, the FPGA can tolerate up to 10 % but this figure should be limited to 2 % to prevent potential errors.

7.2 Interrupt line

A direct digital line exists between the SEPT instrument and the SEP processor (SEPT-E-LATCHUP and SEPT-NS-LATCHUP). This line is used for interrupt notification (see section 8.2).

7.3 Command structure: parameters and arguments

All commands consist of an 8-bit pattern. Up to 3 bits in this pattern can be used as **parameters**, for addressing purposes (PDFE or telescope) and configuration. When a command consists only of a single byte, it is said to have no arguments. Some commands, such as cConfPDFE, have **arguments**. These arguments consist of one or several bytes sent after the 8-bit pattern command. It is assumed that there is at most 1.8 ms between the receipt of a command byte and subsequent argument on the input interface, otherwise a time-out response (rTimeOut, see appendix A) will be generated and the transmission will be aborted.

A command response always contains the command itself. This feature enables to check that the SEPT FPGA has properly received the command. Consequently, before the next command is sent in a command sequence, the SEP processor shall always check that the previous command has been properly echoed. In the case of a non-properly echoed command the action to be taken is still TBD.

7.4 BREAK response

In addition to transmitting and receiving bytes, the serial interface can also generate a break code on the occurrence of an interrupt. This is done by transmitting a zero start bit, one byte with the data filled all zero, two stop bits being zero and an additional zero bit to violate the nominal protocol.
The break signal is sent nearly simultaneously with the assertion of the external interrupt signal, only delayed by any ongoing byte transmission.

Depending on the capabilities of the SEP processor, either the break signal or the interrupt line can be used[2].

7.5 Communication errors

The following table lists the response issued by the SEPT FPGA whenever a problem occurs at the communication level.

rUnknown	Send back 00000011 whenever an unknown command is sent
rTimeOut	Send back 00001111 whenever a time out has occurred while waiting for an argument.

Table 4 Communication troubleshooting response

Whenever a rUnknown and rTimeOut is encountered by the SEP processor, the cRstComm should be sent (TBC) and a TBD action should be taken.

8 Status & Interruption

8.1 Description

The status of the instrument can be described by a certain number of bits contained in the interrupt register:

Bit 0	Event propagation enabled on PDFE 0 and 1 (set to 1 when PDFE operational)
Bit 1	Event propagation enabled on PDFE 2 and 3 (set to 1 when PDFE operational)
Bit 2	Time Alarm interrupt, latched
Bit 3	Saturation interrupt on PDFE 0 and 1, latched
Bit 4	Saturation interrupt on PDFE 2 and 3, latched
Bit 5	Calibration interrupt, latched
Bit 6	PDFE 0 or 1 error or latchup during measurement
Bit 7	PDFE 2 or 3 error or latchup during measurement
Bit 8	PDFE 0 configuration error, latched
Bit 9	PDFE 1 configuration error, latched
Bit 10	PDFE 2 configuration error, latched
Bit 11	PDFE 3 configuration error, latched
Bit 12	PDFE 0 or 1 analogue latchup, latched
Bit 13	PDFE 0 or 1 digital latchup, latched
Bit 14	PDFE 2 or 3 analogue latchup, latched
Bit 15	PDFE 2 or 3 digital latchup, latched

Table 5 Interrupt register

[2] so far we have requested a digital line since we didn't know if the BREAK signal would be supported by the SEP UART.

The whole register is accessible through the `cClearIrq` command. This command also clears all the latched interruption bits in the interrupt register.

Note: The cStatPDFE command gives access to the current PDFE status bits (from bit 8 to bit 15) unlatched, however this command will not be used.

8.2 Interrupt notification

An external interrupt is generated:

- When the alarm timer reaches the preset alarm time
- On the saturation of an event counter (for each telescope)
- On the completion of a test generator sequence[3] (TBC)
- On the detection of a configuration error in a PDFE
- On the detection of a latchup on the analogue or digital power supply to a PDFE pair.

The interrupt is notified by:

- Sending of a BREAK message from the FPGA to the SEP processor
- Assertion of the interrupt digital line.

In normal operation, only timer interrupts will occur.

[3] In AD1, the test generator sequence is called calibration. Here we use “calibration” in reference to the calibration mode described in section 16.

9 Operational modes

9.1 Settings Look Up Table

A lookup table should be stored in the mass memory of the SEP processor. It shall contain all settings needed to properly operate the SEPT instrument and the binning parameters for the beacon mode (see 12.2). The LUT can be divided into two parts:

- LUT_SETTINGS
- LUT_BEACON

The following settings are needed (see AD3 for more details):

Name	Description	Size (bits)
ACC_TIME	Accumulation time	16
G_PDFE0-SEPT-E	Conversion gain adjustment PDFE0-SEPT-E	5
G_PDFE1-SEPT-E	Conversion gain adjustment PDFE1-SEPT-E	5
G_PDFE2-SEPT-E	Conversion gain adjustment PDFE2-SEPT-E	5
G_PDFE3-SEPT-E	Conversion gain adjustment PDFE3-SEPT-E	5
G_PDFE0-SEPT-NS	Conversion gain adjustment PDFE0-SEPT-NS	5
G_PDFE1-SEPT-NS	Conversion gain adjustment PDFE1-SEPT-NS	5
G_PDFE2-SEPT-NS	Conversion gain adjustment PDFE2-SEPT-NS	5
G_PDFE3-SEPT-NS	Conversion gain adjustment PDFE3-SEPT-NS	5
ML_PDFE0-SEPT-E	Main event detection level PDFE0-SEPT-E	8
ML_PDFE1-SEPT-E	Main event detection level PDFE1-SEPT-E	8
ML_PDFE2-SEPT-E	Main event detection level PDFE2-SEPT-E	8
ML_PDFE3-SEPT-E	Main event detection level PDFE3-SEPT-E	8
ML_ PDFE0-SEPT-NS	Main event detection level PDFE0-SEPT-NS	8
ML_ PDFE1-SEPT-NS	Main event detection level PDFE1-SEPT-NS	8
ML_ PDFE2-SEPT-NS	Main event detection level PDFE2-SEPT-NS	8
ML_PDFE3-SEPT-NS	Main event detection level PDFE3-SEPT-NS	8
CL_PDFE0-SEPT-E	Coincidence event detection level PDFE0-SEPT-E	8
CL_ PDFE1-SEPT-E	Coincidence event detection level PDFE1-SEPT-E	8
CL_ PDFE2-SEPT-E	Coincidence event detection level PDFE2-SEPT-E	8
CL_ PDFE3-SEPT-E	Coincidence event detection level PDFE3-SEPT-E	8
CL_ PDFE0-SEPT-NS	Coincidence event detection level PDFE0-SEPT-NS	8
CL_ PDFE1-SEPT-NS	Coincidence event detection level PDFE1-SEPT-NS	8
CL_ PDFE2-SEPT-NS	Coincidence event detection level PDFE2-SEPT-NS	8
CL_ PDFE3-SEPT-NS	Coincidence event detection level PDFE3-SEPT-NS	8

Table 6 LUT_SETTINGS

The values stored in the LUT_SETTINGS will be used by the cConfPDFE and cSetTimer commands.

The LUT_BEACON shall contain the binning parameters for the beacon mode. The binning parameters are related to Table 14 and should be stored as 5 bit values with the following naming.

Name	Default value
Electron_bin1	1
Electron_bin2	5
Electron_bin3	8
Electron_bin4	13
Electron_bin5	17
Ion_bin1	1
Ion_bin2	8
Ion_bin3	20
Ion_bin4	30
Ion_bin5	31

Table 7 LUT_BEACON

The lookup table shall be able to be modified by tele-commands from ground control.
The size of the LUT_SETTINGS is 184 bits, the size of the LUT_BEACON is 50 bits. The whole LUT is consequently 234 bits long.

9.2 Nominal Mode

This mode will correspond to 99.9% of the mission. It consists of the accumulation of the 4 buffers (per SEPT subsystem) during ACC_TIME and the reading of the buffers, the PDFE working in full anti-coincidence mode. HK values will also be read at the end of each accumulation.

The accumulation duration is based on the internal timer of the FPGA.
The binning of the energy is logarithmic and is done internally (32 bins) according to Table 15.
The nominal mode is an “endless” repetition of the series of commands described in Table 8.
It is assumed that the “Nominal Configuration sequence” described in section 10.3 has been initially performed.
The following table describes the series of commands and events in the case where no error occurs (else refer to section 11)

Series 1			
step	**Command**	**Bit pattern +arguments**	**Response (+ received command)**
0	cGetSingle	01001000	Selection of PDFE0 for single counter. A counter value is still returned but not used
1	cStartRun	01100100	
2	Reception of a BREAK signal or assertion of the interrupt digital line		
3	cClearIrq	01110000	Interrupt register with Bit 2 set to 1= timer interrupt
4	Cread32	10110000	PDFE 0 counters
5	Cread32	10110001	PDFE 1 counters
6	Cread32	10110010	PDFE 2 counters
7	Cread32	10110011	PDFE 3 counters
8	cConfPDFE	10010000+First byte:110xxxxx (xxxxx= G_ PDFE0-SEPT-E Second byte: ML_ PDFE0-SEPT-E Third byte: CL_ PDFE0-SEPT-E	
9	cGetHK	01000000	HK_CS0 (1 byte), HK_GR0 (1 byte), HK_CS1 (1 byte), HK_GR1

			(1 byte)
10	cConfPDFE	10010000+First byte:100xxxxx (xxxxx= G_ PDFE0-SEPT-E Second byte: ML_ PDFE0-SEPT-E Third byte: CL_ PDFE0-SEPT-E	
11	cConfPDFE	10010001+First byte:110xxxxx (xxxxx= G_ PDFE1-SEPT-E Second byte: ML_ PDFE1-SEPT-E Third byte: CL_ PDFE1-SEPT-E	
12	cGetHK	01000001	HK_T (4 values)
13	cConfPDFE	10010001+First byte:100xxxxx (xxxxx= G_ PDFE1-SEPT-E Second byte: ML_ PDFE1-SEPT-E Third byte: CL_ PDFE1-SEPT-E	
14	cConfPDFE	10010010+First byte:110xxxxx (xxxxx= G_ PDFE2-SEPT-E Second byte: ML_ PDFE2-SEPT-E Third byte: CL_ PDFE2-SEPT-E	
15	cGetHK	01000010	HK_CS2 (1 byte), HK_GR2 (1 byte), HK_CS3 (1 byte), HK_GR3 (1 byte)
16	cConfPDFE	10010001+First byte:100xxxxx (xxxxx= G_ PDFE2-SEPT-E Second byte: ML_ PDFE2-SEPT-E Third byte: CL_ PDFE2-SEPT-E	
17	cGetSingle	01001000	Return single event counter of the PDF0, main channel.
Series 2			
Same as series 1 except for steps 0 and 17: command is 01001100: Return single event counter of the PDF0, coincidence channel.			
Series 3			
Same as series 1 except for steps 0 and 17: the command is step 17: command is 01001001: Return single event counter of the PDF1, main channel.			
Series 4			
Same as series 1 except for steps 0 and 17: command is 01001101: Return single event counter of the PDF1, coincidence channel.			
Series 5			
Same as series 1 except for steps 0 and 17: command is 01001010: Return single event counter of the PDF2, main channel.			
Series 6			

Same as series 1 except for steps 0 and 17: command is 01001110: Return single event counter of the PDF2, main channel.
Series 7
Same as series 1 except for steps 0 and 17: command is 01001011: Return single event counter of the PDF3, main channel.
Series 8
Same as series 1 except for steps 0 and 17: command is 0100111: Return single event counter of the PDF3, coincidence channel.

Table 8: Nominal mode command/response series

Step 8, 11 and 14 configure the corresponding PDFE in ADC mode, steps 10, 13 and 16 put them back in observation mode.
Note: the so called « beacon mode » corresponds to a special binning performed by the SEP processor and is based on the data produced in the nominal mode.

9.3 Calibration Mode

This mode occurs once a month during some hours. The difference with the previous mode resides only in the configuration of the instrument, which will be set to coincidence mode between two center segments of a telescope and in anticoincidence with the corresponding guard ring. Only the penetrating particles will be recorded.
Consequently once the “calibration configuration” sequence has been carried out, Table 8 sequencing can be used.

9.4 Test Generator Mode

TBD.
Once every 3 months for some minutes. This mode is still to be defined at the FPGA level.

9.5 Timing

The precise timing of the start of the accumulation is important for the SEPT instrument. The accumulation time will be internally handled by the FPGA. ACC_TIME will be set so that the duration between 2 consecutive accumulation starts (corresponding to SEP sending cSTartRun commands) is exactly 60 seconds (within 100 ms, TBC). It means that there will be a waiting state of TBD ms before the beginning of an accumulation (see Figure 3) to enable synchronisation.
Time tagging shall be performed for each SEPT science data packet in accordance with the general scheme adopted for the SEP instrument.

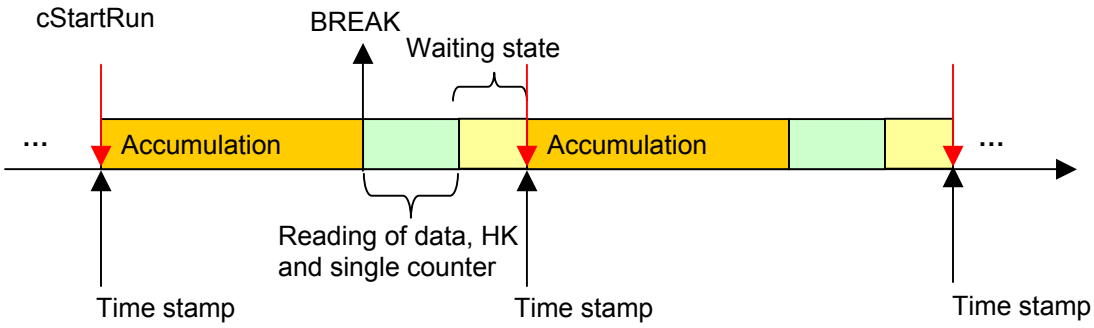

Figure 3 Timing diagram (not to scale)

10 Pre/Post operation Sequences

These sequences are used to configure or power cycle the PDFEs as well as to set up the different operational modes.

10.1 Initialization sequence

After switch-on of the power lines of the SEPT instrument the initialization sequence should be used.

Step	Command	Bit pattern	Description
1	cRstComm	00010010	Reset serial communication
2	cRstFPGA	00010001	Reset FPGA

Table 9: Initialization sequence

10.2 PDFE power-on sequence

This sequence is used whenever the instrument has been initialized.

Step	Command	Bit pattern	Description
1	cPwrPDFE	10000011	Power on PDFEs
2	cDrvPDFE	10000111	Drive outputs to PDFEs
3	cEnPDFE	10001100	PDFE in acquisition mode
4	cCtrlPDFE	10001100	PDFE in digital mode

Table 10: Command sequence to power-up PDFE

10.3 Nominal Configuration Sequence

The following sequence applied to a SEPT-E unit (the sequence for SEPT-NS is easily deducted).

#	Command	Bit pattern	Arguments	Description
1	cConfPDFE	10010000	First byte:100xxxxx (xxxxx= G_ PDFE0-SEPT-E Second byte: ML_ PDFE0-SEPT-E Third byte: CL_ PDFE0-SEPT-E	Configuration of PDFE 0
2	cConfFiltr	00110010		Set the filter mode for PDF0 in FPGA
3	cInitCntr	10101000		Initialize counter for PDFE 0
4	CConfPDFE	10010001	First byte:100xxxxx (xxxxx= G_ PDFE1-SEPT-E Second byte: ML_ PDFE1-SEPT-E Third byte: CL_ PDFE1-SEPT-E	Configuration of PDFE 1
5	cConfFiltr	00110110		Set the filter mode for PDF1 in FPGA
6	cInitCntr	10101001		Initialize counter for PDFE 1
7	CConfPDFE	10010010	First byte:100xxxxx (xxxxx= G_ PDFE2-SEPT-E	Configuration of PDFE 2

			Second byte: ML_ PDFE2-SEPT-E Third byte: CL_ PDFE2-SEPT-E	
8	cConfFiltr	00111010		Set the filter mode for PDF2 in FPGA
9	cInitCntr	10101010		Initialize counter for PDFE 2
10	CConfPDFE	10010011	First byte:100xxxxx (xxxxx= G_ PDFE3-SEPT-E Second byte: ML_ PDFE3-SEPT-E Third byte: CL_ PDFE3-SEPT-E	Configuration of PDFE 3
11	cConfFiltr	00111110		Set the filter mode for PDF3 in FPGA
12	cInitCntr	10101011		Initialize counter for PDFE 3
13	cSetTimer	11010000		

Table 11: Nominal configuration sequence

10.4 Calibration Configuration Sequence

The following sequence applied to a SEPT-E unit (the sequence for SEPT-NS is easily deducted). The difference with the nominal configuration sequence is in the coincidence/anticoincidence configuration (cConfPDFE command).

#	Command	Bit pattern	Arguments	Description
1	cConfPDFE	10010000	First byte:101xxxxx (xxxxx= G_ PDFE0-SEPT-E Second byte: ML_ PDFE0-SEPT-E Third byte: CL_ PDFE0-SEPT-E	Configuration of PDFE 0
2	cConfFiltr	00110011		Set the filter mode for PDF0 in FPGA
3	cInitCntr	10101000		Initialize counter for PDFE 0
4	CConfPDFE	10010001	First byte:101xxxxx (xxxxx= G_ PDFE1-SEPT-E Second byte: ML_ PDFE1-SEPT-E Third byte: CL_ PDFE1-SEPT-E	Configuration of PDFE 1
5	cConfFiltr	00110111		Set the filter mode for PDF1 in FPGA
6	cInitCntr	10101001		Initialize counter for PDFE 1
7	CConfPDFE	10010010	First byte:101xxxxx (xxxxx= G_ PDFE2-SEPT-E Second byte: ML_ PDFE2-SEPT-E Third byte: CL_ PDFE2-SEPT-E	Configuration of PDFE 2
8	cConfFiltr	00111011		Set the filter mode for PDF2 in FPGA
9	cInitCntr	10101010		Initialize counter for PDFE 2
10	CConfPDFE	10010011	First byte:101xxxxx (xxxxx= G_ PDFE3-SEPT-E Second byte: ML_ PDFE3-SEPT-E Third byte: CL_ PDFE3-SEPT-E	Configuration of PDFE 3
11	cConfFiltr	00111111		Set the filter mode

				for PDF3 in FPGA
12	cInitCntr	10101011		Initialize counter for PDFE 3
13	cSetTimer	11010000		

Table 12: Configuration sequence

10.5 Test Generator Configuration Sequence

TBD

10.6 Commissioning Sequence

TBD (Use cInitCntr with bit 5 to 1: PDFE number; page; counter address…..)

10.7 Emergency Switch-off Sequence

TBD

10.8 PDFE Power-off Sequence

The following sequence should be used prior to switch-off the power lines of the SEPT unit.

Step	Command	Bit pattern	Description
1	cEnPDFE	10001100	Low power mode for pdfe
2	CDrvPDFE	10000100	outputs to PDFEs in high impedance
3	CPwrPDFE	10000000	Power off PDFEs

Table 13 PDFE power-off sequence

11 Reaction to interrupts

Whenever an interruption is detected a cClearIrq command should be sent to the SEPT instrument. The subsequent received interrupt register will enable the SEP processor to determine what type of interrupts occurred.

11.1 Datation of interrupts

During an accumulation, it is possible to read the timer value at the occurrence of an interrupt such as latchup, PDFE configuration error or event counter saturation. Irrespectively of the type of event, only the first one will lead to the dating, one per telescope.

11.2 Status word

A status word will be sent together with the data and HK values. This status word will consist of 5 bytes :

- Field A (bytes 1 and 2): interrupt register (obtained tvia the cClearIrq command)
- Field B (bytes 3 and 4): time of the counter saturation, PDFE configuration error or latchup (valid only during accumulation) when occurred.
- Field C (byte 5): Single counter address (3 bits)+ operational mode (3 bits)+ 2 spare (11 by default)
    - o PDFE 0 single counter: 000
    - o PDFE 1 single counter: 001
    - o ….
    - o Nominal mode: 000
    - o Calibration mode: 010
    - o Test generator: 100
    - o Ex:01010011: single counter PDFE1, test generator mode

The status word is valid from step 1 to step 11 of a series as defined in Table 8.

11.3 Interrupts during measurement modes

Only the first interrupt which occurs between step 1 and step 11 of each series (see Table 8) is reported in the status word (for one SEPT unit).

11.3.1 Timer interrupt

The timer will only be used to obtain an accurate accumulation period. Consequently any timer interrupt will signify the end of the current accumulation. The status word will then consist of:

- Field A: interrupt register (obtained in step 3 of Table 8)
- Field B: ACC_TIME

if no other interrupt has occurred during the accumulation.

11.3.2 Saturation interrupt

The cReadDate command shall be sent to the SEPT unit. If no interrupt has already occurred, the bytes 1 and 2 of the response shall be used for the field B of the current status word if saturation occurs on PDFE 0 or 1 (telescope A), bytes 3 and 4 in case of PDFE 2 or 3 (telescope B).

11.3.3 PDFE configuration error

The cReadDate command shall be sent to the SEPT unit. If no interrupt has already occurred, the bytes 1 and 2 of the response should be used for the field B of the current status word if a configuration error occurs on PDFE 0 or 1 (telescope A), bytes 3 and 4 in case of PDFE 2 or 3.
After reception of the subsequent timer interrupt, the PDFE power-off sequence should be started followed by the PDFE power-on sequence and eventually the configuration sequence needed to restore the mode which was active before interrupt (TBC).

11.3.4 Latchup interrupt during accumulation

The cReadDate command shall be sent to the SEPT unit. If no interrupt has already occurred, the bytes 1 and 2 of the response should be kept for the field B of the current status word if a latchup occurs on PDFE 0 or 1 (telescope A), bytes 3 and 4 in case of PDFE 2 or 3 (telescope B).
If a latchup occurs on one telescope, it will be immediately switched off by the FPGA. The subsequent switch-on should be made ONLY by a dedicated command from ground control.

11.3.5 Latchup or error configuration out of the accumulation period

If a configuration error or a latchup occurs outside of the accumulation period, it should be reported in the current status word if no interrupt (except timer) has occurred before. The field A shall then contain the updated status register and the field B set to 0000000000000000. Subsequent actions are the same as presented in the previous subsections.

11.4 Latchup/Configuration error during Pre/post operation sequences

TBD.

12 Data Processing requirements

12.1 Nominal mode/Calibration mode/Test generator mode

In these three modes, the data received by the SEP processor are in the form of 32 counters of 24 bits per PDFE. Each 24 bits value should be compressed to a 12-bit representation (logarithm representation with mantissa in 8 bits, “Hidden Leading One Notation” and exponent on 4 bits). Besides, HK_T should be extracted from the housekeeping stream and averaged or snapshot[4] for operational heater control[5].

12.2 Beacon mode

The data received by the SEP processor are in the form of 32 counters of 24 bits per PDFE. The different channel (energy/particle type/direction) should be summed up as shown in Table 14. The different values should then be compressed on a 16 bit word (format TBD).

Species	Energy window				Directions
	E1	Index	E2	Index	
Electrons (PDFE 0 and 2)	0.02	1	0.05	4	4 separate
	0.05	5	0.1	7	4 summed
	0.1	8	0.2	12	4 summed
	0.2	13	0.4	17	4 separate
Ions (PDFE 1 and 3)	0.02	1	0.1	7	4 separate
(mostly	0.1	8	0.5	19	4 summed
protons)	0.5	20	1.9	30	4 summed
	1.9	30	31	NA	4 separate

Table 14 Beacon mode channels definition

The indexes refer to the Table 15. Each channel shall have a 1-bit status to signify invalid data (1 when overflow or non-nominal status).

[4] The 4 values of the temperature are derived from FPGA hardware constraints. Only one can be taken or the average of the four.
[5] The format of HK_T will be specified later.

13 Data rate

The following figures are valid for one set of SEPT-E and SEPT-NS, they are based on a 60 seconds time resolution (ACC_TIME=60s-ε, ε TBD) for a normal operation (no error).

13.1 Nominal mode

Data	Total Number of bits
8 x 32 bins, 12 bits per bin	3072
18 Housekeeping values, 8 bits	144
2 single counters, 23 bits each	46
2 single counter addresses, 3 bits each	6
LUT_SETTINGS	184
Status word, 40 bits per unit	80

The total is 3532 bits, so 58.9 bit/s.

13.2 Calibration mode

Data	Total Number of bits
8 x 32 bins, 12 bits per bin	3072
18 Housekeeping values, 8 bits	144
2 single counters, 23 bits each	46
2 single counter addresses, 3 bits each	6
LUT_SETTINGS	184
Status word, 40 bits per unit	80

The total is 3532 bits, so 58.9 bit/s.

13.3 Test generator mode

Data	Total Number of bits
8 x 32 bins, 12 bits per bin	3072
18 Housekeeping values, 8 bits	144
2 single counters, 23 bits each	46
2 single counter addresses, 3 bits each	6
LUT_SETTINGS	184
Status word, 40 bits per unit	80

The total is 3532 bits, so 58.9 bit/s.

13.4 Beacon mode

Data	Total Number of bits
20 channels, 16 bit each	320
1 status bit per channel	20

The total is 340 bits, so 5.7 bit/s

14 Appendix A: FPGA commands

14.1 Command parameter definition

Symbol	Meaning	Examples
UU	PDFE Index	00 -> PDFE0 01 -> PDFE1 10 -> PDFE2 11 -> PDFE3
PP	Telescope	00 -> No telescope 01 -> Telescope B 10 -> Telescope A 11 -> Telescope A + B
-	Configuration bits	0 -> disable 1 -> enable

The following tables list the existing commands, the parameters are represented according to the definition given in previous table

14.2 Commands without arguments

Command	**Bit Pattern**	**Description**
cGetId	00010100	Get part identification
cRstComm	00010010	Reset communication
cRstFPGA	00010001	Reset FPGA
cClearIrq	01110000	Read & Clear Interrupt
cStatPDFE	10010100	Read PDFE status
cReadTimer	11010001	Read Timer value
cReadDate	11010010	Read dating value
cGetHK	010000UU	ADC Housekeeping (the ADC of each PDFE is used to digitize HK signals)
cConfFiltr	0011UU--	Configure event filters
cGetSingle	01001-UU	Single counter: all detected counts on the addressed PDFE
cRead256	101101UU	Read & clear the counter of the corresponding addressed PDFE with linear binning
cRead32	101100UU	Read & clear the counter of the corresponding addressed PDFE with 32 log binning
cStartRun	01100---	Start measurements

cPwrPDFE	100000PP	Power PDFE
cGetSingle	01001-UU	Returns the value of the single counter used for measuring all events on teh detector
cCtrlPDFE	100011PP	Control PDFEs
cEnPDFE	100010PP	Enable PDFEs
cDrvPDFE	100001PP	Drive outputs of PDFE
cInitCntr	10101-UU	Initialise 256 bin counters
cStopRun	01101000	Stop measurements

14.3 Commands with arguments

Command	**Bit Pattern**	**Argument(s)**	**Description**
cConfPDFE	100100UU	3 configuration bytes	Configuration of the PDFEs
cConfCntr	101000--	2 bytes	Set mode & page
cConfCal	111-----	3 bytes	Configuration for the test generator mode
cSetTimer	11010000		

The cConfDAC command is not used.

15 Appendix B FPGA 32 bin table

The following table shows the exponential bin boundaries used in the FPGA and the corresponding energy values for a maximum energy of 2.2 MeV. The 32 counters of 24 bits are related to this energy binning. The counter 0 gathers all the counts with energy between 0 and 17.25 keV, counter 1 gathers all the counts with energy between 17.25 and 25.88 and so on….

Index	Energy (keV)
-1	0
0	17.2549
1	25.88235
2	34.5098
3	43.13726
4	51.76471
5	60.39216
6	77.64706
7	94.90196
8	112.1569
9	129.4118
10	155.2941

11	181.1765
12	207.0588
13	241.5686
14	276.0784
15	310.5882
16	353.7255
17	405.4902
18	457.2549
19	517.6471
20	586.6667
21	664.3137
22	741.9608
23	836.8627
24	949.0196
25	1069.804
26	1199.216
27	1354.51
28	1518.431
29	1708.235
30	1915.294
31	>2200

Table 15 Exponential binning table