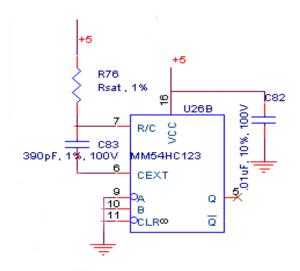
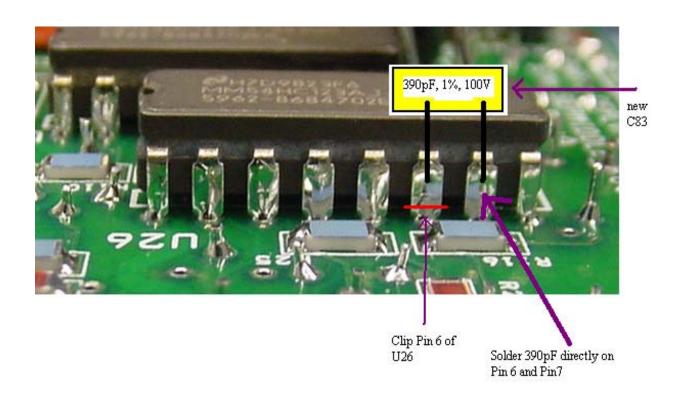
STEREO IMPACT SEP LVPS MIDDLE BOARD		2/26/2004
Requesting Engineer:	Approved by:	···
Date:	Date:	
Date.	Date.	

STEREO IMPACT SEP LVPS FM1 MIDDLE BOARD REPAIR INSTRUCTIONS

1. U26 Pin6 connected to +5V (PFR-1004)

U26 pin6 (CEXT) must be only connected to 390pF capacitor (C83). The line connected was named +5V on the schematic. Therefore the layout generating software has connected the line to +5V. C83 must be removed and a new capacitor (CK05) must be installed. The value of the capacitor remains the same.

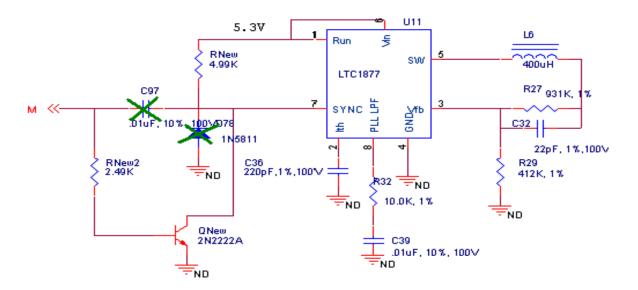




2. LTC1877 SYNC SIGNAL

LTC1877 Sync signal (Pin 7) should not receive negative voltages. In order to prevent negative voltages at SYNC node, a transistor will be installed instead of a Schottky Barrier diode (D78 and D80).

2.1 D78 and U11 repair Instructions



Remove C97

Completed By:

Date:

Remove D78

Completed By:

Date:

Install 2N2222A Pin 1 to ground (anode pad of D78).

Completed By:

Date:

Install 2N2222A pin 3 to D78 cathode location.

Completed By:

Date:

• Connect a 2.49K Ω (RNew2) resistor to the base of 2N2222A transistor. RNC50H2491DS

Completed By:

Date:

D/C:

• Connect other side of the 2.49K Ω to C97 where it connects to signal M.

Completed By:

Date:

 Connect a 4.99KΩ (Rnew) resistor from C97 (SYNC side) to C26 + side which corresponds to 5.3V.

Completed By:

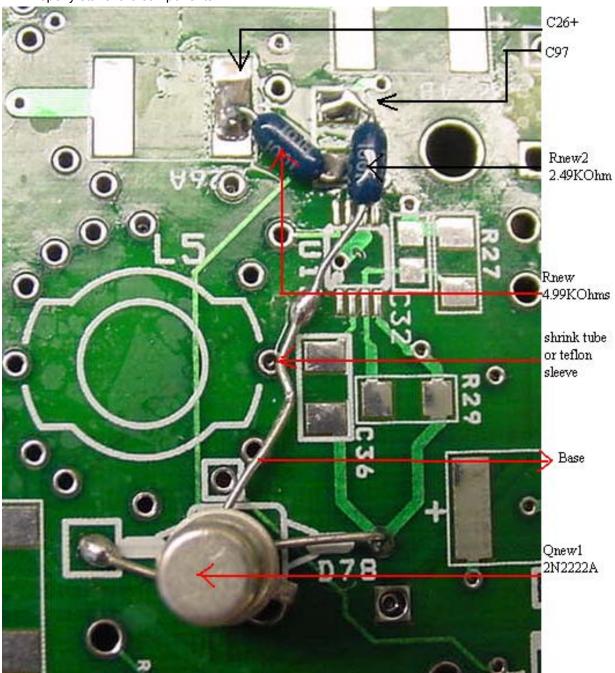
Date:

D/C:

Use shrink tube or Teflon sleeves to cover any exposed leads.

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Date:	Date:	

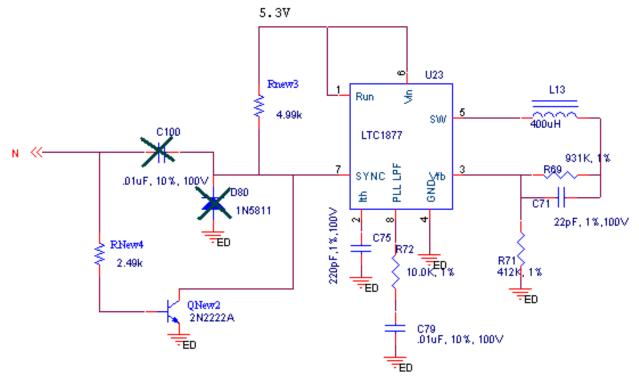
• Properly stake the components.



Date:

Date:

2.2 D80 and U23 repair instructions:



Approved by: ____

Remove C100

Completed By:

Date:

Remove D80

Completed By:

Date:

Install 2N2222A Pin 1 to ground (D80 anode pad location)

Completed By:

Date:

Install 2N2222A pin 3 to D80 cathode location.

Completed By:

Date:

Connect a 2.49KΩ (Rnew4) resistor to the base of 2N2222A transistor. (RNC50H2491DS)

Completed By:

Date:

D/C:

• Connect other side of the 2.49K Ω (Rnew4) to C100 where it connects to signal N.

Completed By:

Date:

 Connect a 4.99KΩ (Rnew3) resistor from C100 (SYNC side) to the via at U23 pin 6. (RNC50H4991DS)

Completed By:

Date:

D/C:

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Requesting Engineer:	Approved by:	
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Date:	Date:	

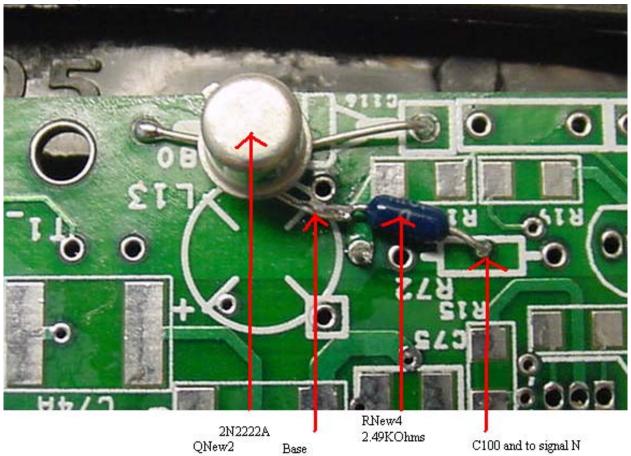
• Use shrink tube or Teflon sleeve where the leads are exposed

Completed By: Date:

• During staking process, stake the new components.

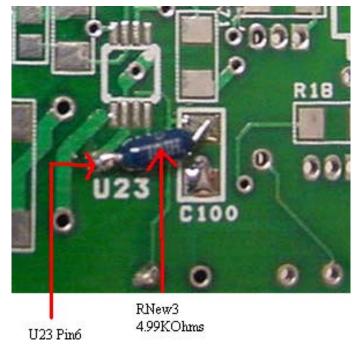
Completed By: Date:

View from top of the SEP LVPS Middle Board:



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Requesting Engineer:	Approved by:	
Date:	Date:	

View from bottom of the SEP LVPS Middle Board:



Approved by: Date:

Approved by: Date: