STEREO IMPACT

PR Numbers: 1xxx=UCB, 2xxx=Caltech/JPL, 3xxx=UMd, 4xxx=GSFC/SEP, 5xxx=GSFC/Mag, 6xxx=CESR, 7xxx=Keil, 8xxx=ESTEC, 9xxx=MPAe

Assembly : HET	**SubAssembly :**
Component/Part Number: FM1	**Serial Number:**
Originator: von Rosenvinge/Wortman	**Organization:** GSFC
Phone : 301-286-9454	**Email :** wortman@LHEApop.gsfc.nasa.gov

Failure Occurred During (Check one √)

X Functional test □ Qualification test □ S/C Integration □ Launch operations

Environment when failure occurred:

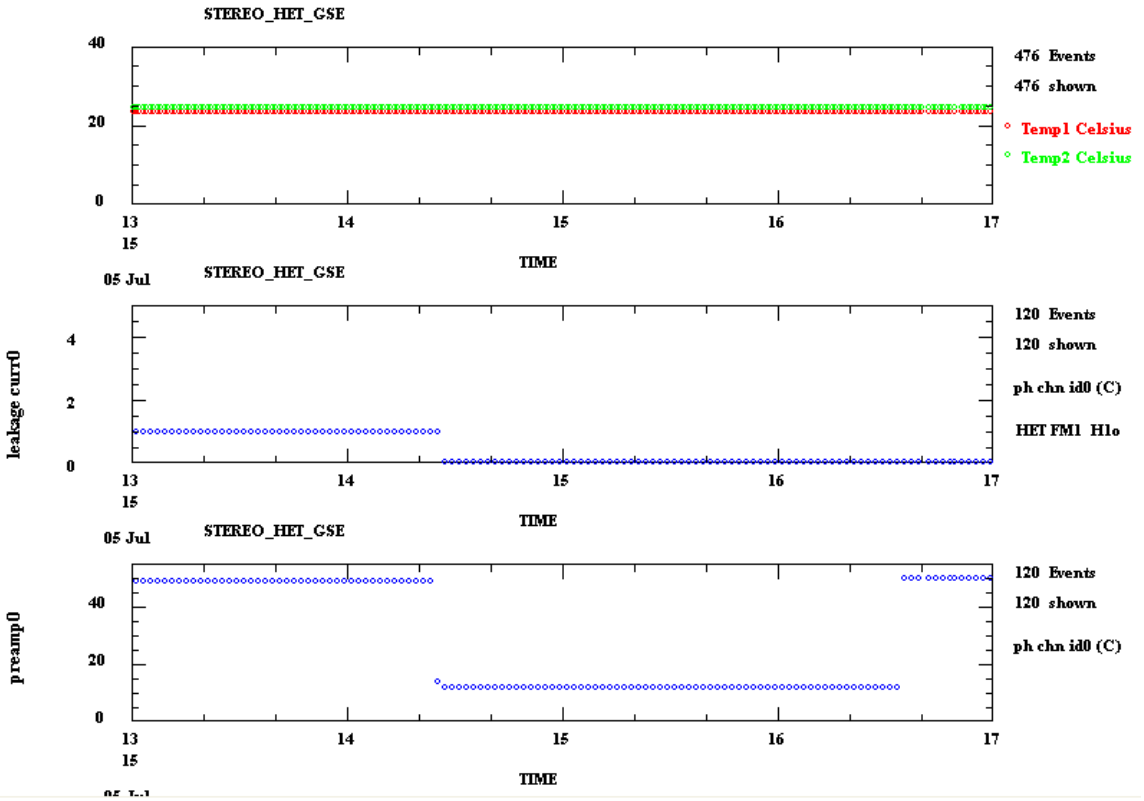
X Ambient □ Vibration □ Shock □ Acoustic
□ Thermal □ Vacuum □ Thermal-Vacuum □ EMI/EMC

Problem Description

A series of HET FM1 comprehensive performance tests (which exercise all the analog detector channels at once) were conducted during the July thermal vacuum and vibration tests by CalTech and GSFC personnel with no anomalies observed. Another comprehensive performance test (which exercises the stimulus pulser to pulse only one analog detector channel at a time) was conducted on 07/15/05 by GSFC where an anomaly was observed.

An anomaly was discovered with the H1 detector while invoking the onboard stimulus pulser on the H1o low and high gain channels. The H1o preamplifier ADC reading decreased from the nominal 50 to 12, which resulted in a voltage reading of 4.75 volts. It should be noted that the firmware attempts to adjust the PHASIC input resistance DAC in order to maintain a reading of 4.0 volts (+- .02 v). It should be noted that this H1 detector was previously tested and normally has a very low leakage current registering below one tenth of a microamp at 40° C. This test was conducted while the temperature was a nominal 23°C. Also, the input resistance DAC dropped from 1 to 0 at the time of this anomaly.

At the time this anomaly was noted, several unsuccessful attempts were made to invoke the firmware's detector leakage current balancing algorithm (by sending a setindacs command) which normally runs at boot up. Once all the detectors (H1i, H1o, H2-H6) were re-enabled, the preamplifier ADC for the H1o detector stabilized at 50 and the current reading of 4.0 volts was established and maintained.



Analyses Performed to Determine Cause

The firmware's leakage current balancing algorithm adjusts the input resistance DACs for the detectors with the intention of causing a 0.3V downward shift of the preamp output. The 0.3-volt shift temporarily moves the preamplifier output voltages into the range for which the buffer amp operates in the linear range. Therefore new input resistance DAC settings are computed for all the detectors. The target for each preamp reading is 50, which corresponds to a preamp output of 4.0 volts. (Full scale is 5.0V, and the preamp ADC reads out in two's complement, so a reading of 0 is full scale and 255 is 0V. The formula is Volts = 5*(256-reading)/256.)

The difference between the actual reading and the target reading of 50 is used to adjust each preamp input resistance DAC setting to move the preamp output voltage to the 4.0V target. However, because the offset has been added back to "undo" the 0.3-volt shift, the actual target for the preamp output voltages is 4.3V. The adjustment computation is set forth below.

The computations described above are performed in a transformed coordinate space. The raw input resistance DAC setting is specified in "N12" format, in which the least significant 5 bits is referred to as N1 and the most significant as N2, with the injected current given by:

current = (1uA)*(N2 + N1*10/256)

However, for ease of computation, another representation, "N3" format, is more convenient. The conversion from "N12" to "N3" is given by:

N3 = [2^16]*N2 + 10*[2^8]*N1 (2)

Hence N3 is a number that is proportional to the injected current and has units of about 2^-16 uA. The algorithm for converting from "N12" format to "N3" format just implements equation (2). To go back the other way, N3 is divided by 2^16 to get N2 and the remainder is divided by 2560 to get N1. (Due to the non-monotonicity of eq (1), there are sometimes two different "N12" format settings that yield about the same injected current, but have N2 different by 1 and N1 different by about 26. This method of going from "N3" back to "N12" picks the setting with the large value of N2.)

The 0.3 Volt offsetting is done in "N3" space by adding or subtracting 9830*Nf, where Nf is the feedback capacitor setting (Cf = Nf*5p). The feedback capacitor setting (either 6 or 12 in the HET detectors) is read from the current detector settings as written to the PHASICs. If the adjustment would be greater than full scale or less than zero, the value is pegged at full scale or zero, respectively. Before being written to the input resistance DAC, the adjusted value is converted back to "N12" space.

The adjustment based on the difference between the measured preamp output and the target value of 50 is also done in "N3" space by an amount:

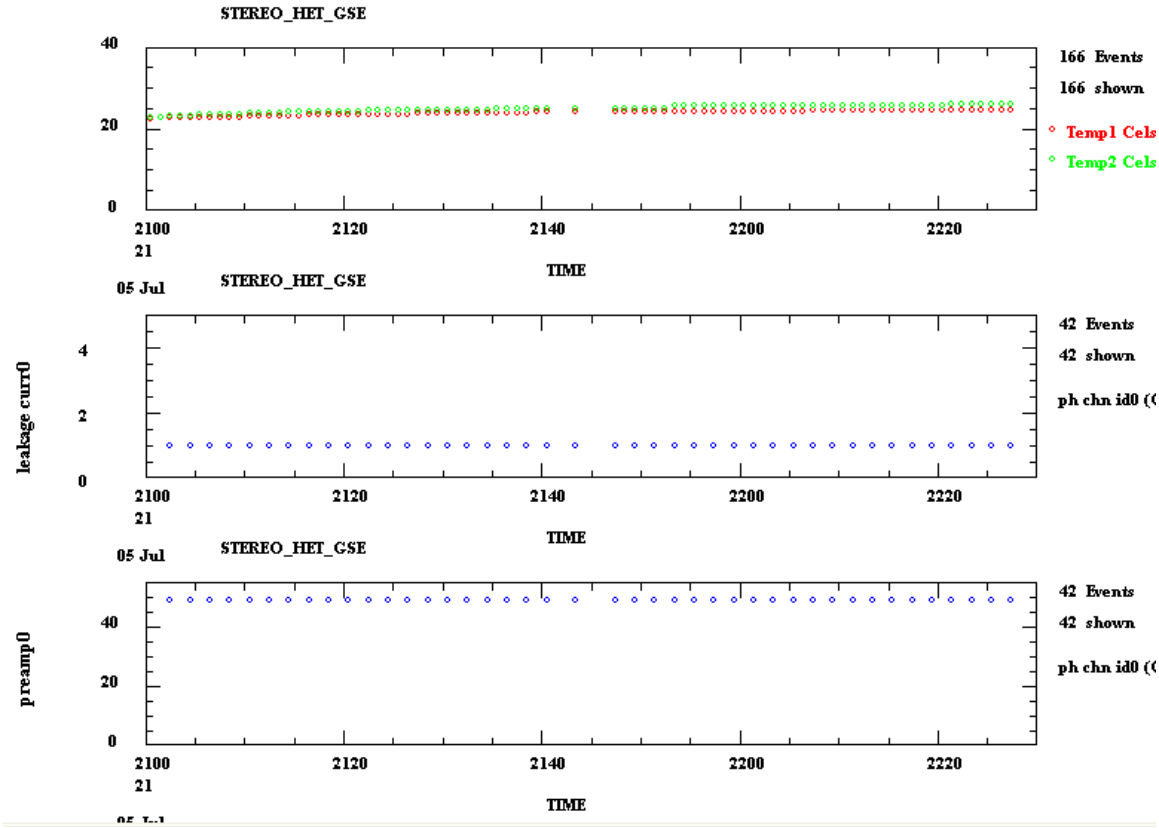
dN3 = (ADCVAL-50)*640*Nf

However, if the absolute value of the difference (ADCVAL-50) is less than 2 (i.e. is 0 or 1) no adjustment is made. Again, care is taken that the adjusted value does not exceed full scale or go lower than zero. The adjusted input resistance DAC setting is saved for the housekeeping telemetry.

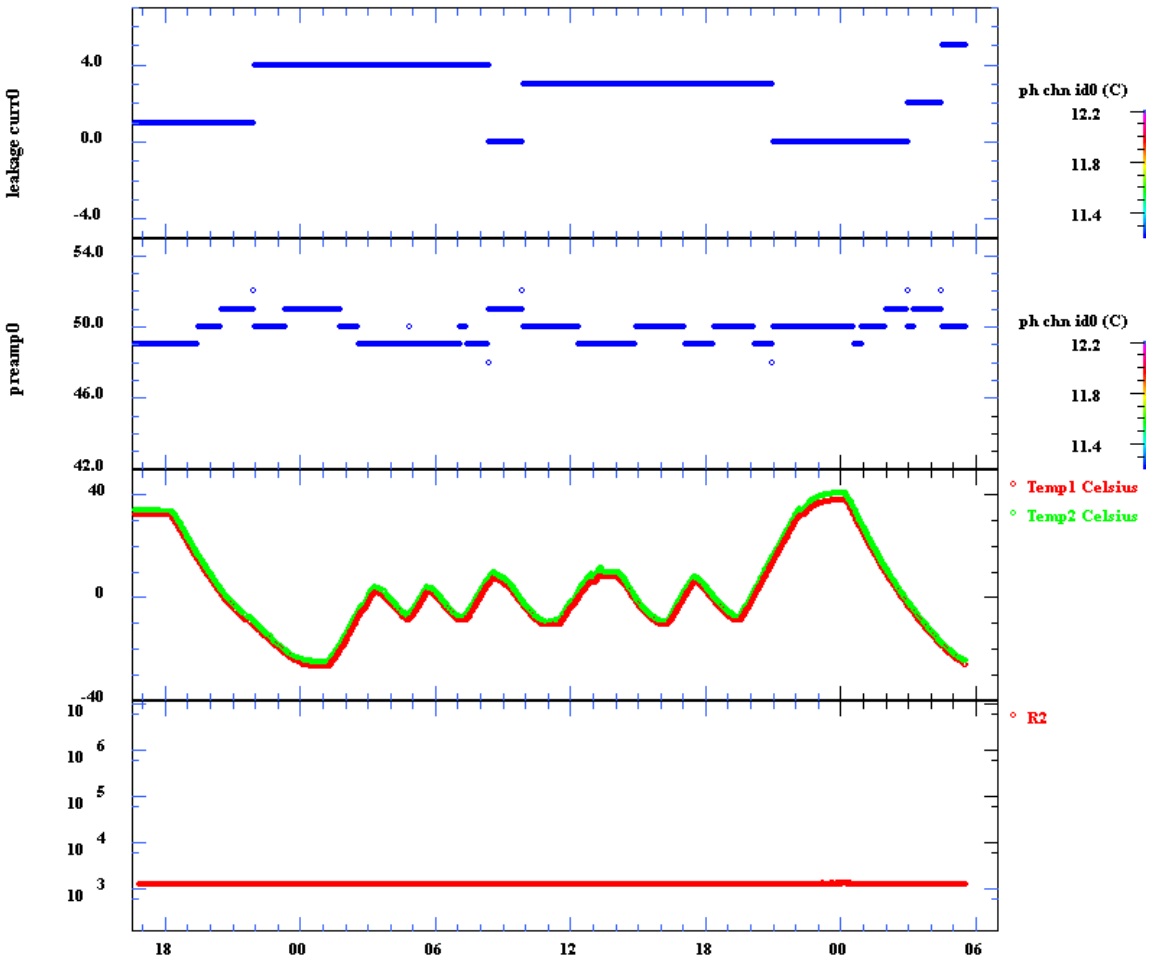
After the leakage current balancing is performed, the new input resistance DAC settings are sent to the PHASICs. The 0.3V offset was already added back in after the ADC readouts, so the operational preamp settings for the next major frame will be targeted to 4.3V.

Several unsuccessful attempts were made by GSFC to recreate this anomaly by pulsing the H1o low and high gain channels.

On July 21, the H1o channel was singly pulsed for over an hour when the temperature was 24°C and the input resistance DAC was constant at 1. The preamplifier ADC also remained constant at 50 to maintain the 4.0 volts (+- .02 v). Thus the earlier problem failed to be reproduced.



On July 23 13:00 to July 25 03:00, the H1o channel was also singly pulsed while temperatures were cycling from -25° to 35°C in thermal vacuum at which time the preamplifier ADC ranged between 48 and 52 to maintain the 4.0 volts (+- .02 v) and the input resistance DAC range was 0 to 5. So again, the original problem failed to reoccur.



Corrective Action/ Resolution

☐Rework ☐ Repair X Use As Is ☐ Scrap

The command logs were reviewed for the time period where the anomaly occurred as follows:

05/07/15 14:19:12
05/07/15 14:20:12
SEP> HET-CMD
HET> 01F801 phacont 0 b 1
HET>
SEP> HET-CMD

HET> 01F901 phacont 0 b 6

The anomaly was caused by an incorrect command (highlighted in red) which caused the software to configure the HET FM1 H1o channel to be turned off completely. The phacont command is used to configure the phasic chip (parameter 1) and the channel (parameter 2) to the value specified in parameter 3 (channel setting). The valid values for parameter 3 of the phacont command are 0, 1, 7, b, and f. The third parameter was inadvertently specified as a 6, an invalid setting for the phacont command. The intended command and parameters should have been tpfbsel 0 b 6. As a result, the software defaulted to a 0 setting which turns the channel off completely. Therefore since the channel was in the off state, this resulted in an ADC preamplifier reading of 12, which when plugged into the GSE leakage current balancing algorithm yields a 4.75 volts (+- .02 v) in the converted housekeeping value readout. Once the phacont command was sent to reenable the channel on the flight unit, the nominal ADC preamplifier reading was read out and the GSE leakage current balancing algorithm yielded a converted housekeeping value 4.0 volts (+- .02 v). The anomaly can be recreated on both HET flight units by sending the phacont command with an invalid setting to any channel yielding the same result. During normal flight mode operations, all channels will be turned on.

Date Action Taken: 01-19-2006 **Retest Results:** N/A

Corrective Action Required/Performed on other Units ☐ Serial Number(s): ___n/a_____

Closure Approvals

Subsystem Lead:	_____	Date:_____
IMPACT Project Manager:	_____	Date _____
IMPACT QA:	_____	Date:_____
NASA IMPACT Instrument Manager:	_____	Date:_____