STEREO IMPACT

PR Numbers: 1xxx=UCB, 2xxx=Caltech/JPL, 3xxx=UMd, 4xxx=GSFC/SEP, 5xxx=GSFC/Mag, 6xxx=CESR, 7xxx=Keil, 8xxx=ESTEC, 9xxx=MPAe

Assembly: SEP	**SubAssembly: SEP Bias Supply**
Component/Part Number:	**Serial Number: FM1**
Originator: Branislav Kecman	**Organization: Caltech**
Phone: (626) 395-4264	**Email: kecman@srl.caltech.edu**

Failure Occurred During (Check one √)

□ Functional test √ Qualification test □ S/C Integration □ Launch operations

Environment when failure occurred:

□ Ambient □ Vibration □ Shock □ Acoustic
□ Thermal □ Vacuum √ Thermal-Vacuum □ EMI/EMC

Problem Description

During thermal balance test on 5/19/2005, at -15 ºC as the temperature rose, SEP Bias Supply collapsed. This was verified externally on a break-out box used for dummy load to replace missing SIT and SEPT sensors. HET and LET detector rates were affected. Power-cycle solved the problem.
During the thermal vacuum test on 7/23/2005, at -15 ºC as the temperature rose, SEP Bias Supply collapsed and self-restored multiple times, as if the control clock signals for the Bias Supply were coming and going. HET and LET detector rates were affected. Power-cycle solved the problem.

Analyses Performed to Determine Cause

7/24/2005 e-mail message (bellow) from Rick Cook summarizes the analyses performed with the SEP Bias Supply designer, Dean Aalami of Space Instruments:

This problem with FM1 bias supplies does raise concern for damage, since housekeeping readings of the voltage monitors show values up to 500 V (HK ADC full scale). However, I did contact Dean Aalami yesterday and learned that the capacitive multiplier is incapable of producing more than about 336 V. Further, this voltage is series regulated down to the actual bias voltage near 175 V (for L3's and HET). We spent some time reviewing the schematics and symptoms to find a possible explanation for the anomaly. Here is a brief summary.

Symptoms include:

1) Both positive and negative bias readings from the housekeeping system were improper for a period of about 4 hours. The values included many consistent with the supplies being turned off alternating on one minute time scales (the housekeeping system sample period) with many near the values appropriate for the supplies turned on.

2) The plot of positive bias voltage showed some evidence of periodicity at about 35 minutes period imposed on the higher frequency behavior, particularly for the few readings above the nominal "supply on" value.

3) While I haven't reviewed the data, the second hand comment is that the detector singles count rates for both LET and HET were unstable during the four hours of anomaly.

4) There was some correlation between the anomalous housekeeping measurements of the positive and negative bias voltages, with the highest positive readings occurring only when the negative readings were near the off state values.

5) After power cycling the problem disappeared.

Observations from the schematics:

6) The positive and negative bias supplies are largely independent, but do share the same low voltage supplies, pc board and shield enclosure.

7) The outputs of the capacitive multipliers, both the positive and negative one, are monitored by resistively dividing down to the 0-5 V range, then buffering the result with op amps. Dean noted that two op-amps have compensation capacitors which might be too small (10 pF) and leave these op-amps prone to oscillation. However, this had not occurred in testing over temp at Space Instruments.
The op-amps share a positive supply voltage, suggesting that coupled oscillation is possible.

8) The buffered outputs travel from the HV bias board to the analog board where they enter the housekeeping multiplexor. All other low voltage and temperature measurements made through this same multiplexor system were normal throughout the four hours.

9) The two capacitive ladder bias generators operate in an open loop fashion, each using a separate clock supplied by the SEP Central MISC ACTEL. The frequency of these clocks is settable by command via the SEP Central MISC, but in our CPT we don't exercise this command capability, but rather these frequencies are initialized to default values at boot and left constant. There is no software within SEP Central that is supposed to routinely update these frequency settings. The only provided mechanism is via explicit command. However a common hardware register at peripheral address 7 is used to hold both of the nine bit digital numbers that set the frequencies, as well as two bits that serve as on/off for each clock.

Discussion:

Given 9) it is reasonable to consider the possibility that a bit flip within SEP Central might have caused data meant for some routinely written peripheral address register to be sent to address 7 rather than the intended address. This could cause the bias supplies to turn on and off erratically, but would not be expected to cause any voltages beyond the normal range that the ladders can produce and, in particular, would not be expected to produce the 500 V readings seen to occasionally occur for the positive supply.

Coupled oscillation of the op-amps that buffer the bias voltage monitors might be able to produce the observed erratic housekeeping readings, including the ones near 500 volt, but would not be expected to actually cause the detector bias to have problems and so cannot explain the erratic detector count rates. (Unless there is some way for an oscillation to couple to the actual detector bias voltages -- which Dean thought unlikely given the layout and impedances.)

Dean considered the possibility of corona near the output of the 300 V ladder. At the output there are four 22 MΩ resistors in series that form the upper part of the resistive divider for the voltage monitor. Corona across one of these might effectively short it out and be able to produce the 500 V readings. However, presumably this explanation requires corona also on the negative supply. That supply normally runs at only about –100 V. One possible mechanism for inducing corona might be the bursting of a small bubble in conformal coat or elsewhere, raising the pressure within the bias shield enclosure. This hypothesis does potentially explain the (so far) one time occurrence and resetting by power cycling.

However, it seems to me that the details seen in the plots of the bias voltages are hard to explain via the corona model. Particularly, the correlations seen between and positive and negative bias readings and the clear 35 minute periodicity and structure in the positive readings look more like what might happen due to a flipped bit that causes wrong data to go to register 7. However, the bit flip theory seems to have trouble explaining the high (500 V) readings. But perhaps the buffer op-amps are responding with overshoot or oscillation as a result of erratic voltages from the multiplier ladders. Maybe we could try to reproduce such behavior in our EM unit.

If the anomaly was somehow due to corona it may be unlikely to repeat. If it was due to a bit flip it probably will repeat, but at an apparently very low rate. If it does repeat during the subsequent T/V testing it was agreed that we would leave the system in the anomalous state to provide an opportunity for debugging. (This seems safe given that FM1 has already experienced four hours of the anomaly and that there seems no way to produce harmful voltages out of the multiplier stacks.)

If the problem was due to corona at the ladder outputs there would be the possibility of damage to the monitor buffer op-amps. These op-amps appeared to work properly after power cycling. The principle function of these op-amps is to provide diagnostic info that allows adjustment by command of the clock frequencies provided to the multiplier ladders. In-flight failure of one or both of these op-amps would cause the loss of diagnostic this info, however other diagnostic info is available to use in setting the clock frequencies -- the detector leakage current measurements which when added together yield the multiplier stack load, at least for the positive stack that supplies LET and HET. I am not sure if there are leakage current measurements available for all the detectors which use the negative stack.

Corrective Action/ Resolution

√ Rework □ Repair □ Use As Is □ Scrap

1. 5/28/2005 Retested FM1 SEP Main Assembly at -10 ºC in thermal chamber at Caltech, but could not reproduce the anomaly. The instrument wasn't able to get colder than -10 C due to the insulation provided by bagging and purging.
2. 7/31/2005 Memory chip replaced on SEP Central Logic Board and it solved the problem (Reference PFR 2014). The FM1 unit passed re-qualification T/V test between 8/8/2005 – 8/11/2005.

Date Action Taken: 5/28/2005 – 7/31/2005 **Retest Results**: Passed

Corrective Action Required/Performed on other Units □ Serial Number(s): N/A

Closure Approvals

Subsystem Lead:	_Branislav Kecman_____	Date:__8/31/05____
IMPACT Project Manager:	_____	Date _____
IMPACT QA:	_____	Date:_____
NASA IMPACT Instrument Manager:	_____	Date:_____