STEREO IMPACT

PROBLEM REPORT
PR-1036
SEP LVPS
2005-02-27

PR Numbers: 1xxx=UCB, 2xxx=Caltech/JPL, 3xxx=UMd, 4xxx=GSFC/SEP, 5xxx=GSFC/Mag, 6xxx=CESR, 7xxx=Keil, 8xxx=ESTEC, 9xxx=MPAe

Assembly : SEP LVPS	**SubAssembly :** Top and Middle Board
Component/Part Number: SEP_TOP_F001 and SEP_Middle_F001	**Serial Number:** FM2 and FM1
Originator: Selda Heavner	**Organization:** U.C. Berkeley
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Failure Occurred During (Check one √)

√ Functional test □ Qualification test □ S/C Integration □ Launch operations

Environment when failure occurred:

√ Ambient □ Vibration □ Shock □ Acoustic
□ Thermal □ Vacuum □ Thermal-Vacuum □ EMI/EMC

Problem Description

SEP LVPS FM2 was intermittently consuming high current at turn-on. The high-current at turn-on did not reach 0.90A which is the recommended current limit for the bench supply. It typically remained at 580-600mA range. The 28V line did not change when the Supply was consuming 580mA and remained at 28.0V. The supply was not left in the high current state for longer than 30 seconds.

Analyses Performed to Determine Cause

SEP ETU Unit was tested using the bench supply from Caltech KIKUSUI PMC35-1A. SEP ETU was turned on and off until the problem was reproduced. When the high-current occurred the switching FETS became extremely hot. The FETs were still functional after leaving the high-current on a long time. Therefore, the problem is with the FET drivers (for the switching FETs that drive the transformers). When the drivers first come on they set their output to high impedance until their supply voltage exceeds some threshold. So the FET gate floats, and depending on leakage currents the FET can turn on providing a low impedance short (through the transformer windings) on the primary regulator. This in turn causes the voltage regulator to go into current limit so the voltage never gets over the turn-on threshold for the FET driver. So the difference between supplies (and between bench supplies that come up slower or faster) is if the leakage current is large enough to charge up the gate before the primary regulator voltage gets high enough to turn on the driver.

The circuit was analyzed to determine if any parts were stressed by this condition. The FETs were the only candidates, and while the duration was probably too short to damage the FETs, they were replaced anyway (Q3, Q6, Q11, Q14, Q22, Q15, Q18, Q20 on the middle board, and Q10, Q12, Q19, and Q21 on the top board).

Corrective Action/ Resolution

√ Rework □ Repair □ Use As Is □ Scrap

100KΩ resistor from the FET gate to ground can hold the FETs off when the driver is in high impedance mode. This solution was incorporated on ETU and the problem could not be reproduced. Figure 1 indicates where the new resistors (Rnew) will be connected for the Top and Middle Board.

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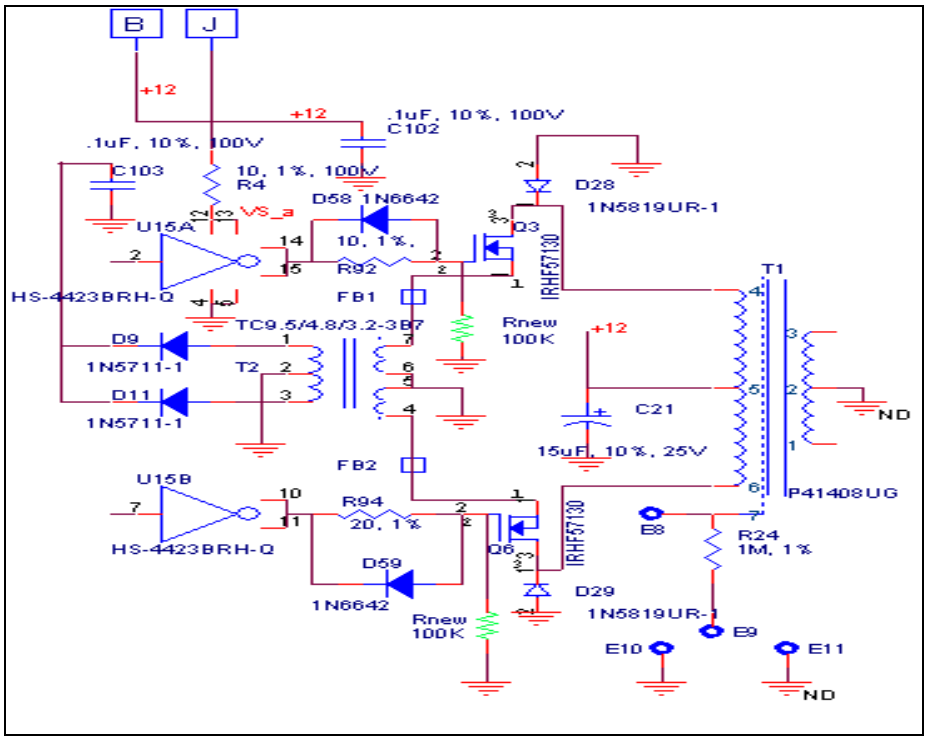
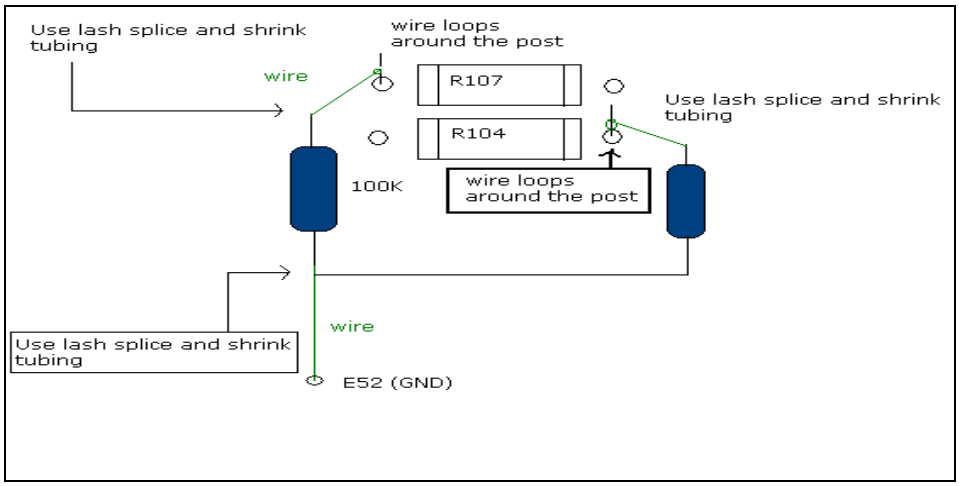


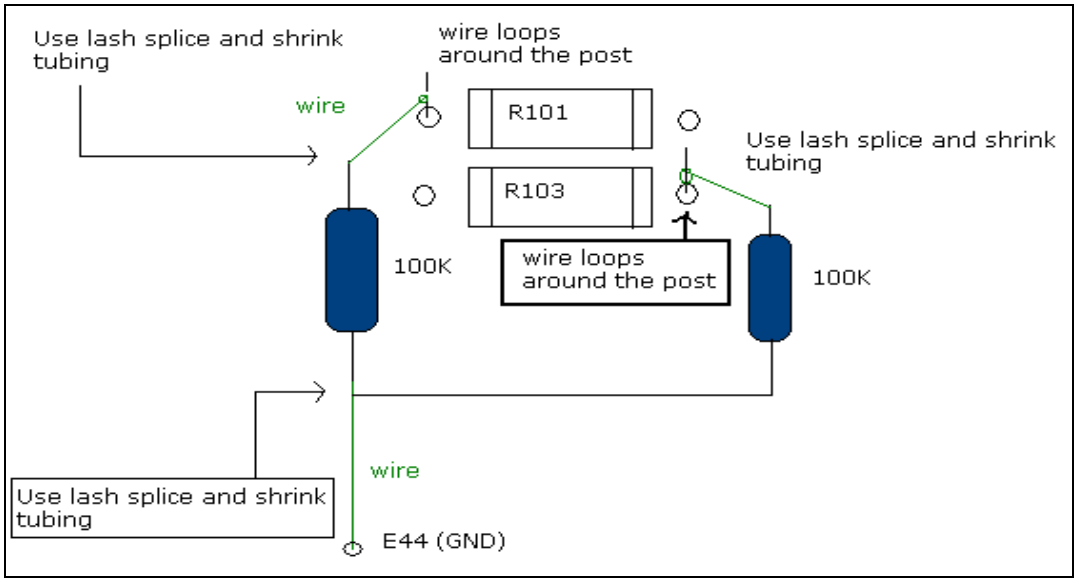
For the Middle Board

1- Connect a small post on R107 (D68 anode side).
2- Connect #24AWG wire on the small post installed.
3- Connect a 100KΩ (RNC50H1003FR) to the wire using lash splice. The wire must be as short as possible. The additional resistors must be close to the corresponding gate drive.
4- Put shrink tubing over where wire and the resistor are soldered.
5- Install a small post on R104 (D66 anode side)
6- Connect #24AWG wire on the small post installed.
7- Connect a 100KΩ (RNC50H1003FR) to the wire using lash splice. The wire must be as short as possible. The additional resistors must be close to the corresponding gate drive
8- Connect the other side of the resistors and #24AWG together using lash splice.
9- Cover the connection with shrink tubing.



10- Connect the wire to E52.
11- Stake the wires and additional resistors.

12- Connect a small post on R101 (D65 anode side).
13- Connect #24AWG wire on the small post installed.
14- Connect a 100KΩ (RNC50H1003FR) to the wire using lash splice. The wire must be as short as possible. The additional resistors must be close to the corresponding gate drive.
15- Put shrink tubing over where wire and the resistor are soldered.
16- Install a small post on R103 (D64 anode side)
17- Connect #24AWG wire on the small post installed.
18- Connect a 100KΩ (RNC50H1003FR) to the wire using lash splice. The wire must be as short as possible. The additional resistors must be close to the corresponding gate drive
19- Connect the other side of the resistors and #24AWG together using lash splice.
20- Cover the connection with shrink tubing.
21- Connect the wire to E44.
22- Stake the wires and additional resistors.



23- Connect a small post on R98 (D62 anode side).
24- Connect #24AWG wire on the small post installed.
25- Connect a 100KΩ (RNC50H1003FR) to the wire using lash splice. The wire must be as short as possible. The additional resistors must be close to the corresponding gate drive.
26- Put shrink tubing over where wire and the resistor are soldered.
27- Install a small post on R95 (D60 anode side)
28- Connect #24AWG wire on the small post installed.
29- Connect a 100KΩ (RNC50H1003FR) to the wire using lash splice. The wire must be as short as possible. The additional resistors must be close to the corresponding gate drive
30- Connect the other side of the resistors and #24AWG together using lash splice.
31- Cover the connection with shrink tubing.
32- Connect the wire to E22.
33- Stake the wires and additional resistors.

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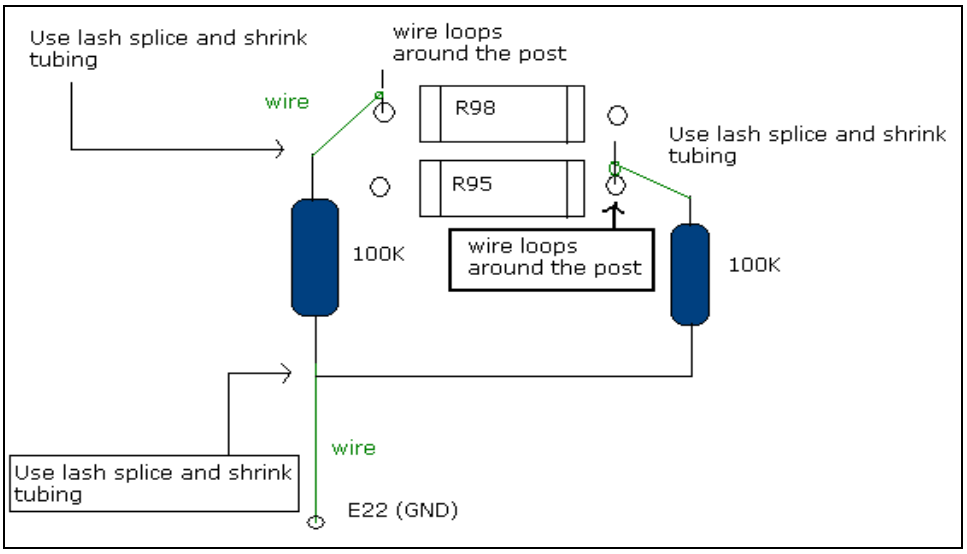
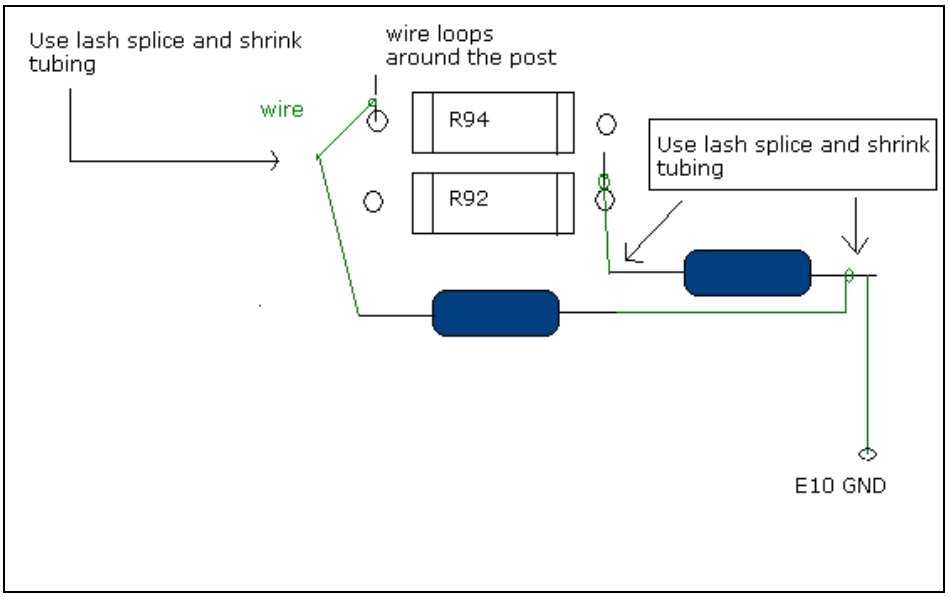


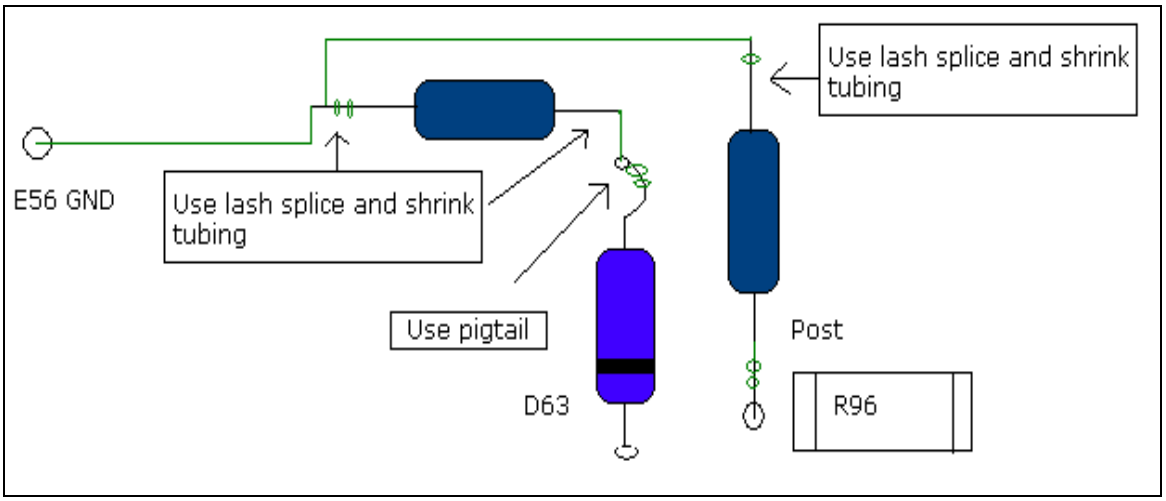
34- Connect a small post on R94 (D59 anode side).
35- Connect #24AWG wire on the small post installed.
36- Connect a 100KΩ (RNC50H1003FR) to the wire using lash splice. The wire must be as short as possible. The additional resistors must be close to the corresponding gate drive.
37- Put shrink tubing over where wire and the resistor are soldered.
38- Install a small post on R92 (D58 anode side)
39- Connect #24AWG wire on the small post installed.
40- Connect a 100KΩ (RNC50H1003FR) to the wire using lash splice. The wire must be as short as possible. The additional resistors must be close to the corresponding gate drive
41- Connect the other side of the resistors and #24AWG together using lash splice.
42- Cover the connection with shrink tubing.
43- Connect the wire to E10
44- Stake the wires and added resistors.



45- Replace Q3, Q6, Q14, Q11, Q22, Q15, Q18 and Q20. (IRHF57130SCS)
46- Coat transistors that were replaced using Uralane 5750.

For the TOP Board

47- Connect a small post on R96 (D61 anode side).
48- Connect #24AWG wire on the small post installed.
49- Connect a 100KΩ (RNC50H1003FR) to the wire using lash splice. The wire must be as short as possible. The additional resistors must be close to the corresponding gate drive.
50- Put shrink tubing over where wire and the resistor are soldered.
51- Remove D63
52- Install new D63 (JANTXV1N6642) with pigtail on its anode side.
53- Connect a wire on the pigtail.
54- Connect a 100KΩ (RNC50H1003FR) to the wire using lash splice
55- Connect the other side of the resistors and #24AWG together using lash splice.
56- Cover the connection with shrink tubing.
57- Connect the wire to E56
58- Stake the wires and added resistors.



59- Remove D67
60- Remove D69
61- Install new D67 (JANTXV1N6642) with pigtail on its anode side
62- Install new D69 (JANTXV1N6642) with pigtail on its anode side
63- Connect a 100KΩ (RNC50H1003FR) to anode of D67 using lash splice.
64- Connect a 100KΩ (RNC50H1003FR) to anode of D69 using lash splice.
65- Connect the other side of the resistors and #24AWG together using lash splice.
66- Cover the connection with shrink tubing.
67- Connect the wire to E32
68- Stake the wires and added resistors using Uralane 5753.
69- Replace Q10, Q12, Q19 and Q21 (IRHF57130SCS)
70- Coat the new transistors with Uralane 5750.

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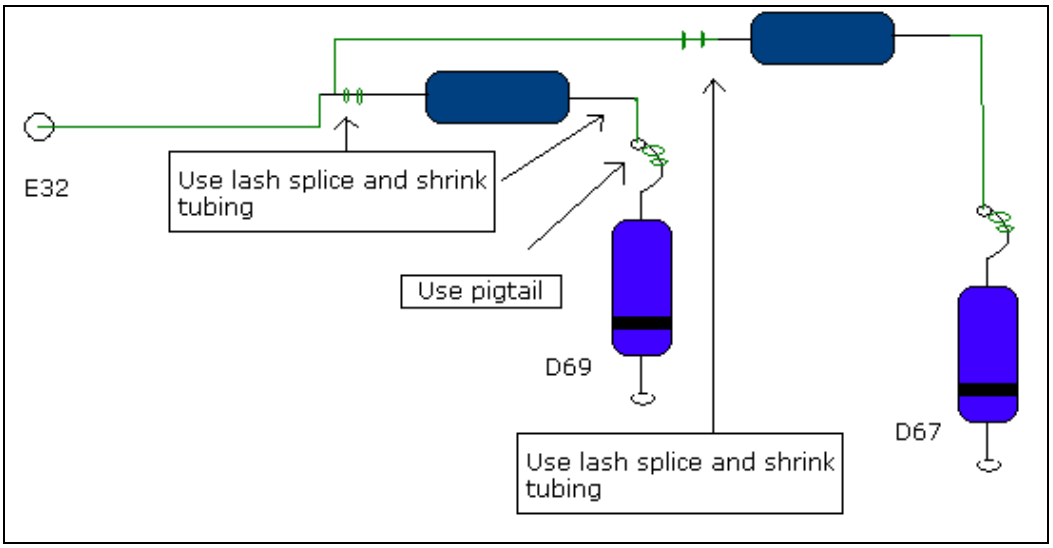

Date Action Taken: _____ **Retest Results**:_____
Corrective Action Required/Performed on other Units : √ Serial Number(s):SEP LVPS ETU

Closure Approvals

Subsystem Lead:	_____	Date:_____
IMPACT Project Manager:	_____	Date _____
IMPACT QA:	_____	Date:_____
NASA IMPACT Instrument Manager:	_____	Date:_____