STEREO IMPACT

PR Numbers: 1xxx=UCB, 2xxx=Caltech/JPL, 3xxx=UMd, 4xxx=GSFC/SEP, 5xxx=GSFC/Mag, 6xxx=CESR, 7xxx=Keil, 8xxx=ESTEC, 9xxx=MPAe

Assembly : SEP LVPS	**SubAssembly :** Middle Board
Component/Part Number: SEP_Middle_F001	**Serial Number:** FM1
Originator: Selda Heavner	**Organization:** U.C. Berkeley
Phone : 510-643-8640	**Email :** selda@ssl.berkeley.edu

Failure Occurred During (Check one √)

v Functional test | Qualification test | S/C Integration | Launch operations

Environment when failure occurred:

v Ambient | Vibration | Shock | Acoustic
Thermal | Vacuum | Thermal-Vacuum | EMI/EMC

Problem Description

During first power-on of the SEP LVPS Middle Board FM1 the no output was observed at pin 12 of MM54HC123A (one-shot).

Analyses Performed to Determine Cause

The layout is inspected. The capacitor C83 is supposed to be connected only to the Rsat and the Pin 6 of the one-shot. However Pin6 of the one-shot (U26) is also connected to Vcc due to an error in layout generating software.

Corrective Action/ Resolution

Rework | v Repair | Use As Is | Scrap

1. Remove C83 (see page 2 of PR-1004 for figures)
2. Remove solder from Pin6 of U26.
3. Using an anti-shock cutter clip Pin 6 of U26 (stake the pad during staking process)
4. Solder a 390pF, 1%, 100V capacitor (CK05) directly onto the chip between pin6 and pin 7 of the one-shot (U26)
   Note: Applying 5V to the MM54HC123A at CEXT is not detrimental to the circuit. CEXT can handle maximum of 6V.

Date Action Taken:____4-28-03_____ **Retest Results**:_____Success_____

Corrective Action Required/Performed on other Units v Serial Number(s): __FM2_____

Closure Approvals

Subsystem Lead: _____ Date:_____
IMPACT Project Manager: _____ Date _____
IMPACT QA: _____ Date:_____
NASA IMPACT Instrument Manager: _____ Date:_____

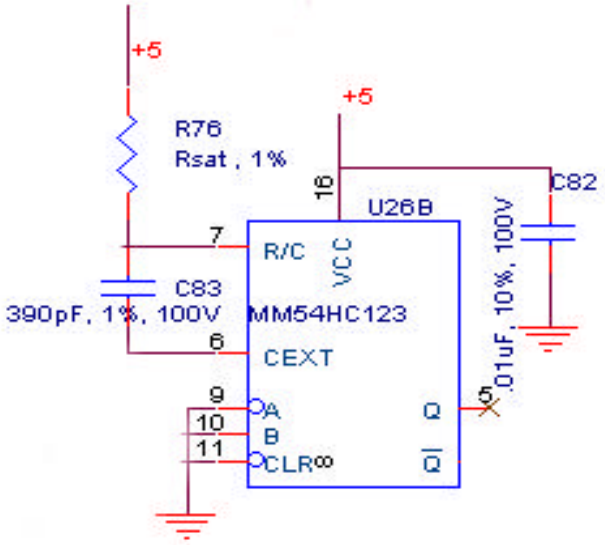

Figure 1: SEP LVPS Middle board Schematic

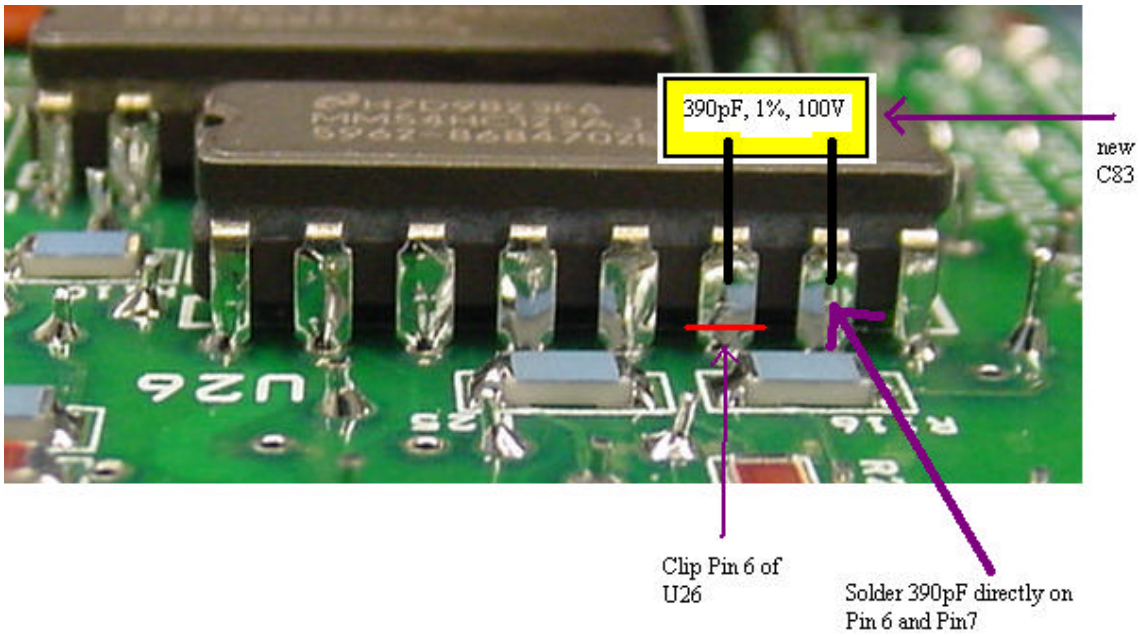

Figure 2: SEP LVPS Middle Board Proposed Solution for PR-1004