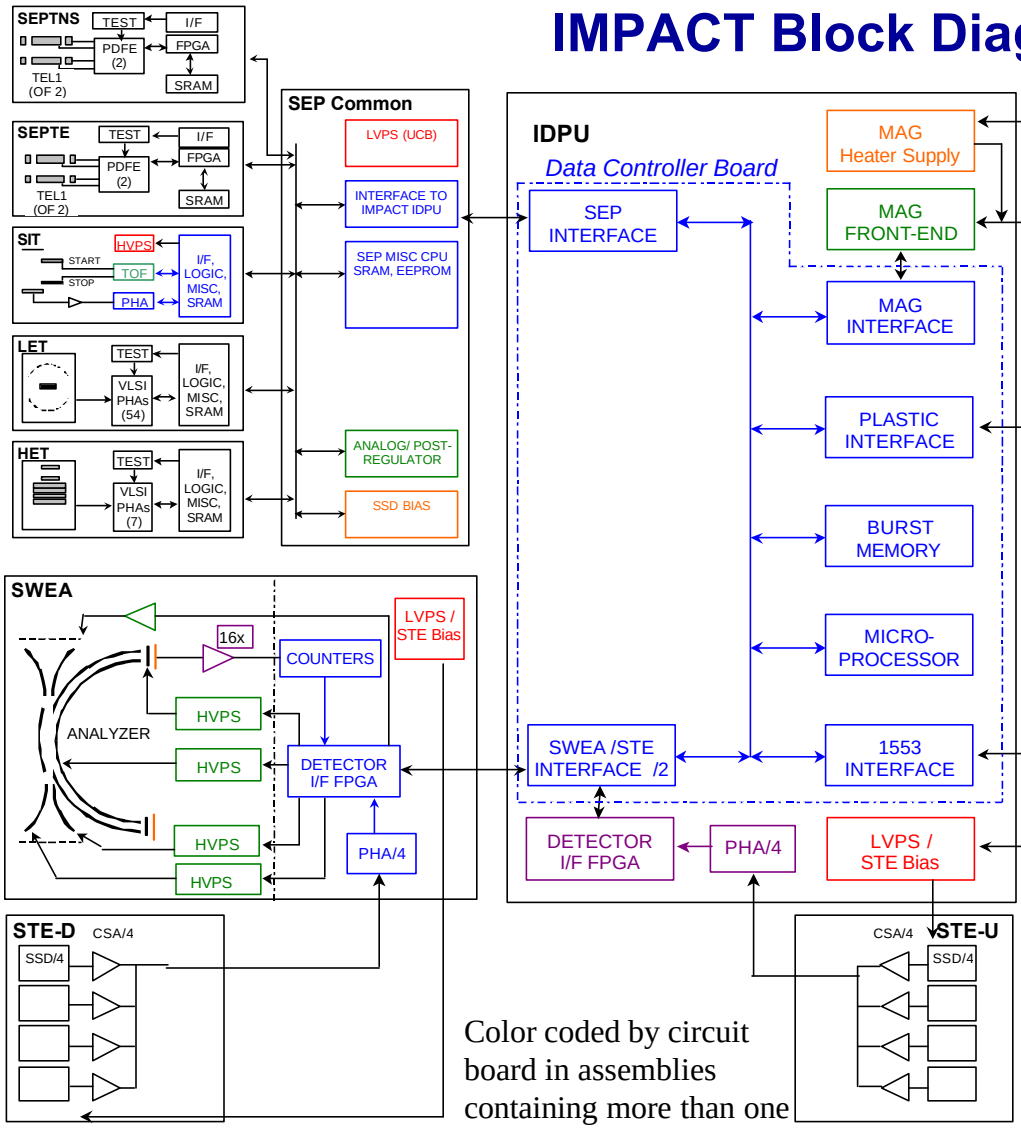
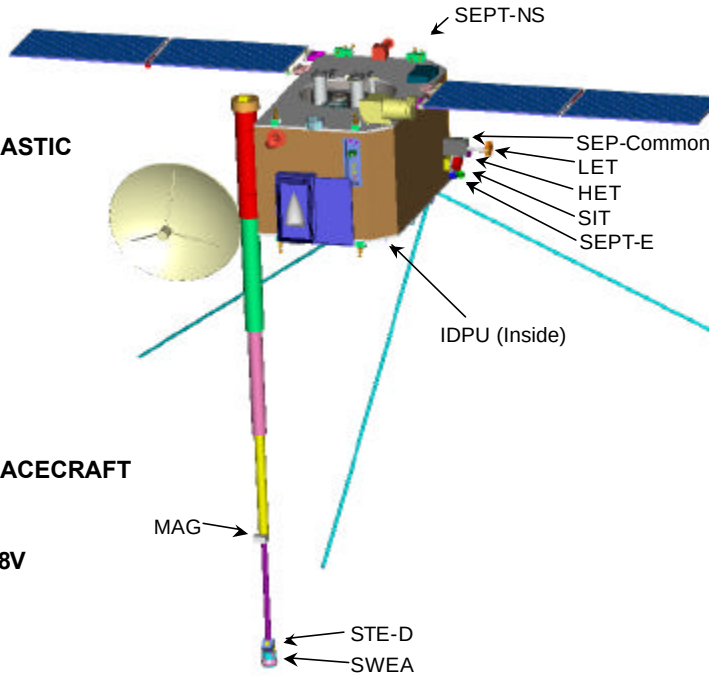
STEREO IMPACT

IMPACT Block Diagram



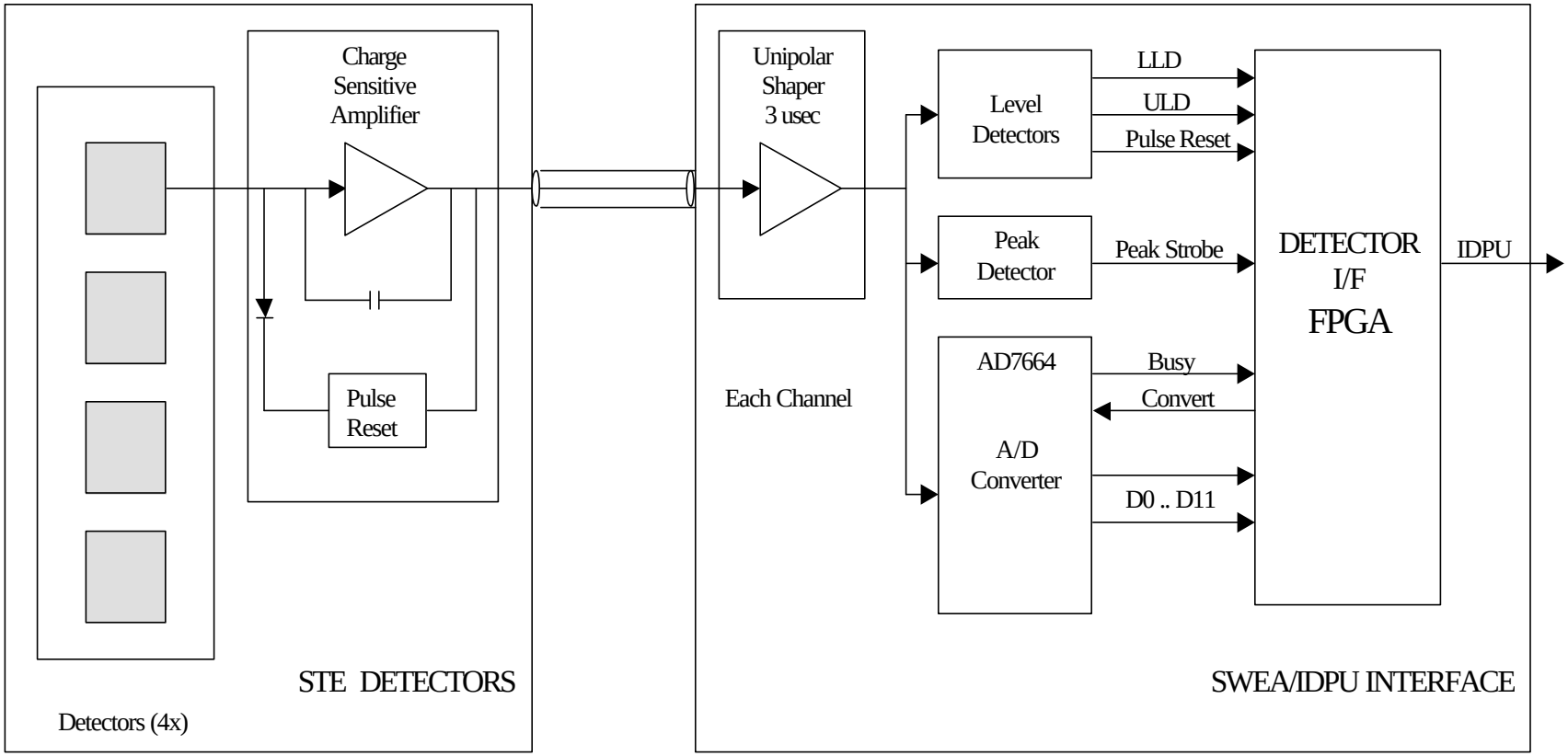


Color coded by circuit board in assemblies containing more than one board.

David Curtis

STEREO IMPACT

STE Signal Chain (one of 4)



STE STATUS

- **DETECTORS AND PREAMP**
  - **DEVELOPED BY LBL**
  - **DETECTORS HAVE HAD PRELIMINARY TESTING TO MEASURE PROPERTIES AND VERIFY CONCEPT**
  - **PREAMP NOISE IS LIMITING FACTOR FOR THRESHOLD DETECTION**
    - **PRESENTLY (~800 ev FWHM) MEETS PROJECT SPECIFICATIONS**
    - **GOAL IS 400-600 Ev**
  - **NOISE INVESTIGATION OF PREMP**
    - **PREDOMINENT SOURCE OF NOISE IS INPUT FET**
    - **SUBSTITUTION OF FETs AND PROTOTYPE PREAMP WITH ALTERNATE FETs AND KNOWN PREAMP**
    - **MODIFY PREAMP LOOP TO EXPOSE SECOND STAGE NOISE**
    - **NOISE CHARACTERISTICS DON'T FIT STANDARD FET NOISE MODELS**
    - **HIGH FREQUENCY 1/F NOISE**
    - **STATE OF ART DUAL GATE FETs**
    - **PREFORMANCE AT ROOM TEMPERATURE**
  - **POSSIBLE IMPROVEMENTS**
    - **ALTERNATE SOURCE OF FETs**
    - **THERMALLY ISOLATE DETECTORS AND FETS FROM REST OF PREAMP TO PROVIDE COLD TEMPERATURE**

SWEA/STE INTERFACE

- **STE SHAPERS AND PHA A/DS**
  - **3 uS UNIPOLAR SHAPER WITH GATED BASELINE RESTORER**
  - **LOW LEVEL INTERFACE TO A/D AND DISCRIMINATORS WITHIN ACTEL FPGA**
  - **PROTOTYPED AND TESTED THROUGH DIGITAL INTERFACE (SIMULATES ACTEL FPGA)**

- **SWEA DACS**
  - **DESIGNED AND PROTOTYPED**
  - **DESIGN CHANGE > UPDATE PROTOTYPE FOR DIFFERENT DAC**
  - **PRELIMINARY SOFTWARE WRITTEN TO TEST DACS**

- **STE DACS**
  - **DESIGNED AND PROTOTYPED**

- **DOOR AND HEATER SWITCHES**
  - **DESIGNED**

- **ACTEL FPGA**
  - **INTERFACES PARTLY DEFINED**