Low Energy Telescope (LET)
SEP-Common Electronics
Status Report

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for the
Caltech, JPL, and GSFC Team

STEREO/IMPACT Meeting
12/14/01

SCALE
0
1
2
3
4
5cm
L1A1
L1A2
L1A3
L1A4
L1A5
L1B1
L1B2
L1B3
L1B4
L1B5
130°
L2B
L3B
L3A
L2A
LET FRONT-END
ELECTRONICS BOARD
30° FOV

LET Silicon Detector Status

- L1 (2 cm^2 area, 20 μm thick, 3-segments, 10 devices for each S/C,)
  - proceeding with baseline approach:
    - 300 μm wafers being etched down to produce 20 μm active area surrounded by thick frame
    - thinning being done by JPL personnel working at UC Berkeley—thinning tests have produced arrays of 2 cm^2 thin areas with good thickness uniformity
    - thinning being done by Micron Semiconductor (England)
    - mask set fabrication is complete and wafer processing has begun
    - vibration test of 3 "pre-prototype" L1 detectors was done with no failures

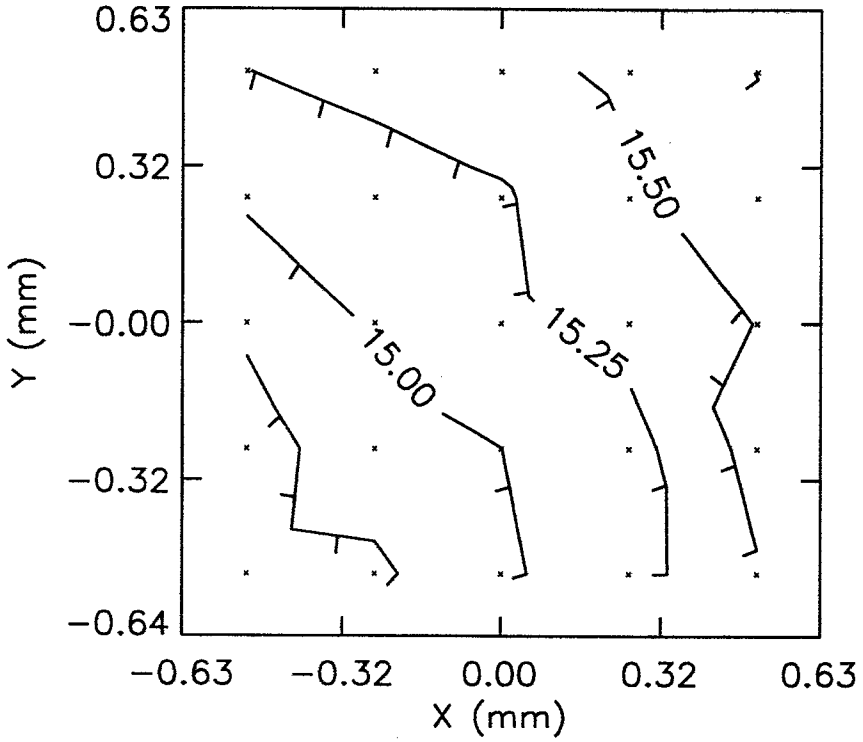
LET Silicon Detector Status (cont.)

- L1 (cont.)
  - backup L1 option is being pursued in case problems are encountered with baseline approach
    - Micron will make prototype L1 using "conventional" approach starting from lapped and polished 20 μm silicon wafers

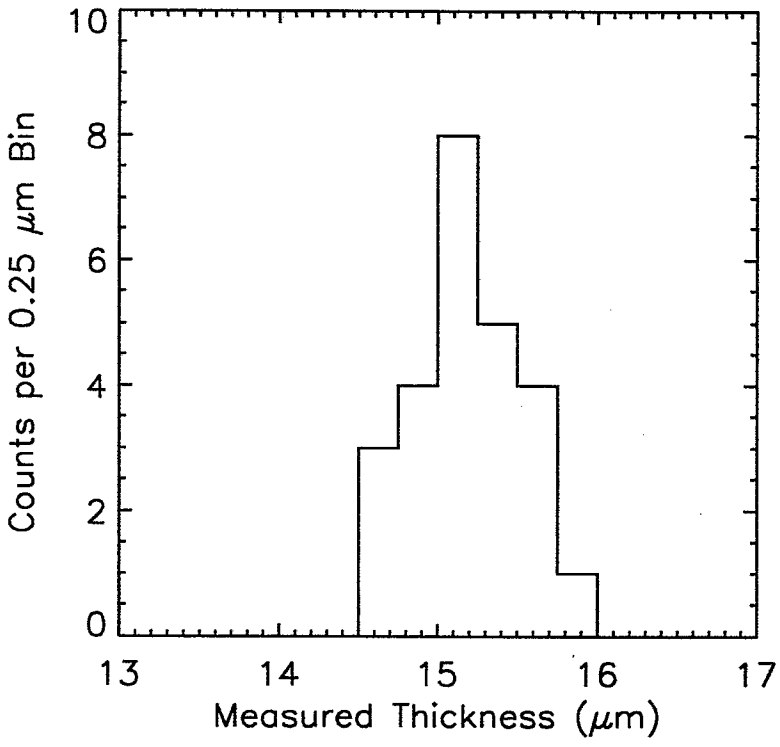
- L2 (10.2 cm^2 area, 50 μm thick, 10 segments, 2 devices for each S/C)

  L3 (15.6 cm^2 area, 1000 μm thick, 2-segments, 2 devices for each S/C)
  - conventional processing by Micron Semiconductor
  - LET and HET share common detector masks, LET portion is complete, mask designs should be sent out for fabrication in December once final corrections are made to H1 and H3 designs

4−inch Si Wafer Thinned by JPL

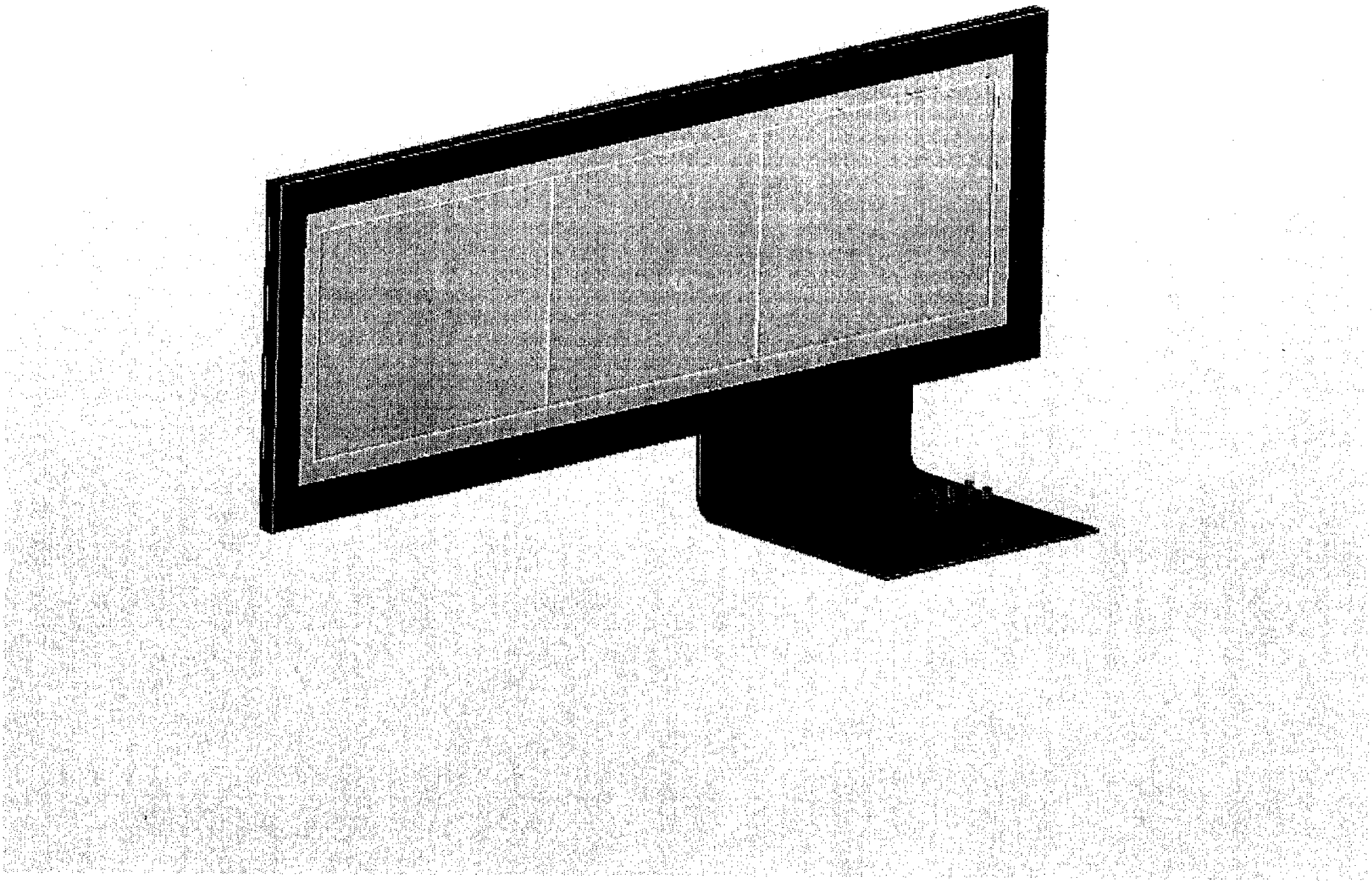


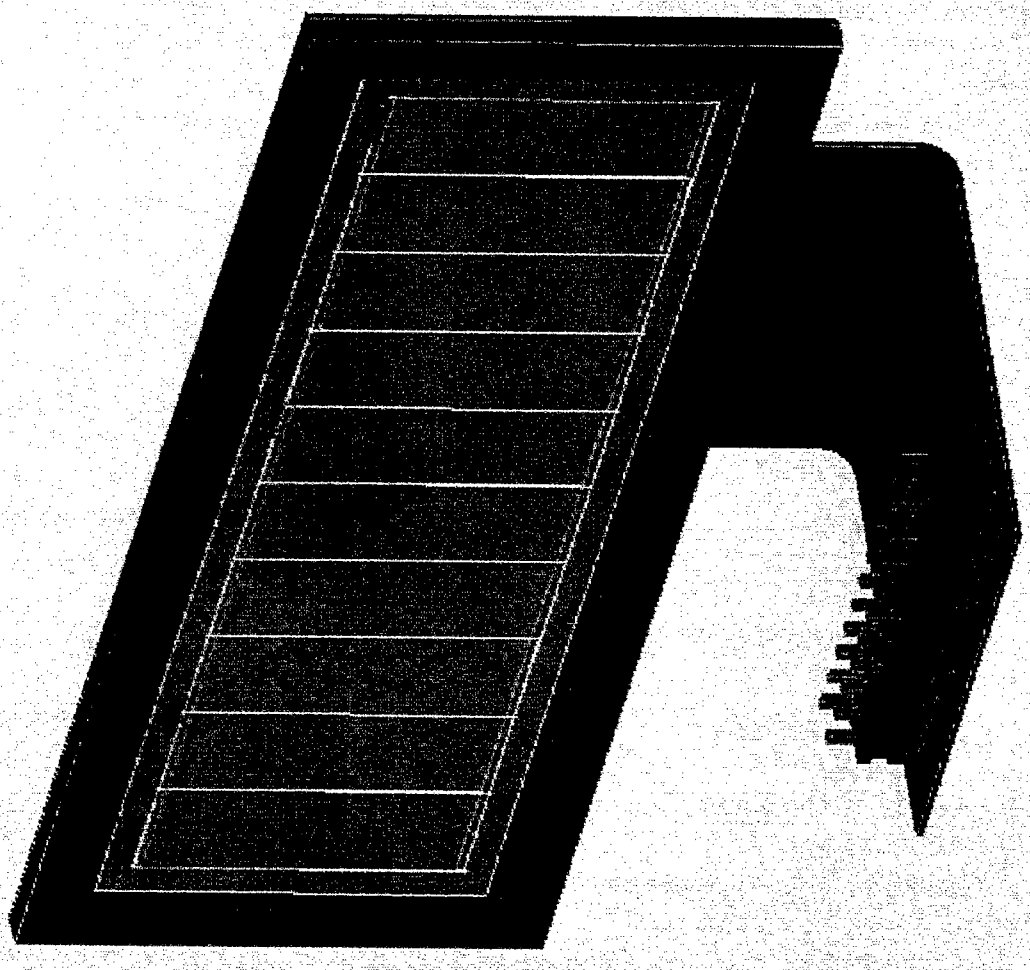
Thickness Contour Map
0.25 μm interval



Thickness Variation:
0.31μm rms

Tue Sep 11 19:12:15 2001 /home/mew/thin_si/alpha_tests/5X5_PROTO/thkmap02.ps





STEREO PHA VLSI STATUS

- Three person team has completed layout of individual sections. Dean and Jill have delivered their layout sections to Rick for edit/integration.

- On track for Jan. 2002 submission.

- Still need cold temperature testing of prototype PHA VLSI.

- Representative layout reviewed by APL. Comments:
- Our guard rings have small gaps (to allow for single poly wires). APL experience is only with no-gap guard rings. New Mexico experience (and physics) indicate the small gaps are ok.
- Our guard rings do not always encircle the "back side" of transistor groupings. APL experience is only with closed rings. We will make modifications to close all rings.
- APL has experienced total dose failure of custom CMOS circuits at as low as a few krad without "edgeless transistors". We are not using edgeless transistors and expect that total dose tolerance will exceed 20 krad. We will test parts for total dose. Fall back is to re-spin with UTMC hardening process add-on to AMI C5N standard process. APL will see if they have any total dose tolerance data for AMI's C5N process.

- HEFT project flight VLSI (recently back from dedicated AMI C5N run) is in test and appears to be working per expectations, validating our design/layout check procedures and AMI interface.

MISC Developments

- At GSFC: Bob Baker has implemented MISCs using Verilog (a VHDL-like logic definition language) and successfully created working MISC systems in both ALTERA and ACTEL FPGAs. The ACTEL version achieves similar good gate utilization and low power dissipation as Caltech's schematic-based designs. The Verilog implementation offers enhanced design portability.

- GSFC has made significant progress in developing MISC software tools for use in HET and SIT, including MISC-resident de-bug monitor and cross-assembler.

- At Caltech: routing success with several MISC versions has removed early concern about possible ACTEL routing difficulty.

- Caltech MISC versions include one for HEFT project implemented in less than one week, containing complete set of application specific logic and i/o, and exercising six of seven available interrupts. This version uses serial boot method and UART operating at 57.6 Kbaud similar to configurations desired for LET, HET and SIT. MISC is in use to operate and collect data from HEFT VLSI readout chip. MISC and forth system are working nicely in a demanding real-world application.

- 54SX72 rad-tolerant ACTEL parts appear on schedule and are now available (in 2.5 and 3.3 V i/o option). Re-spin required for 5 V i/o option.

LET/SEP-Central Flight Software

- Software Development Plan approved by SEP team and delivered to Project
  - Includes resource requirements, build plan, schedule, etc.
- Software Requirements Document is in preparation
- Preliminary LET data packet format spec. is written, being iterated by SEP team
- Protocol for interface between SEP sensors and Sep-Central MISC is being discussed

SEP resources: Mass [g] 12/14/01

Component	Present	PDR
SIT sensor & door	500	500
SIT elec. boards & wiring	370	370
SIT HVPS	160	160
SIT encl. & hdwr	200	200
SIT subtotal:	**1230**	**1230**
SEPT-NS	520	520
SEPT-E	520	520
SEPT subtotal:	**1040**	**1040**
LET det. & housing	515	515
LET electronics	235	235
LET subtotal:	**750**	**750**
HET det. & housing	500	500
HET electronics	160	160
HET subtotal:	**660**	**660**
Cent. elec. encl. & hdwr	1500	1500
El. boards, shields, harness	1090	1090
Central electr. subtotal:	**2590**	**2590**
SEPT-NS bracket	270	270
LET bracket	600	600
SEP bracket	N/A	N/A
SEP total:	**7140**	**7140**
SEPT-NS Ahead harness (1.7 m)	185	185
SEPT-NS Behind harness (2.9 m)	293	293
SEPT-E Ahead harness (0.4 m)	73	73
SEPT-E Behind harness (2.3 m)	240	240
Thermal blankets	120	120
SEP Ahead total:	**7518**	**7518**
SEP Behind total:	**7793**	**7793**

SEP resources: Power [mW] 12/14/01

Component	Present	PDR
SIT HVPS & energy el.	473	473
TOF CFD (from STEP)	680	680
MISC @ 4 MHz	120	120
SIT subtotal:	**1273**	**1273**
SEPT	**1005**	**1005**
LET VLSI	486	486
HK ADC	65	65
MISC @ 8 MHz	223	223
LET subtotal:	**774**	**774**
HET VLSI	63	63
HK ADC	65	65
MISC @ 8 MHz	223	223
HET subtotal:	**351**	**351**
Analog/Post-reg	210	210
Logic (MISC @ 4MHz)	120	120
SSD bias supply	200 @ +20 C *	200 @ +20 C *
Central electr. sub.:	**530**	**530**
LVPS (65% eff.)	2118	2118
SEP total:	**6051**	**6051**

* SSD bias supply capable of consuming 313 mW @ +35 C & end of detector life.

SEP resources: **Data rate [bit/s]** **12/14/01**

Component	Present	PDR~
SIT	417.6	243.6
SEPT	69.6	69.6
LET	556.8	348
HET	208.8	139.2
Central electronics	0	0
SEP total:	**1252.8**	**800.4**

Notes:

SEP will send 2088 data bits/packet in 36 packets/minute as follows:
LET - 16, SIT - 12, HET - 6, SEPT - 2. Packet header (11 bits) excluded.

Beacon data: 1 packet/minute (separate from above).

HK data: 1 packet/minute (separate from above).

~ After distributing SEPT extras and quantifying packages.

LET Functional Testing

- Built in test pulsers will test electronics, including gains, offsets, linearity, and noise
- Background runs produce low-level single detector count rates that test if detectors are connected. They do not produce multi-detector events. To test all 30 L1 detectors may take hours, possibly an overnight run. L2 and L3 are easier to test.
- An alpha-particle source could potentially test all L1 detectors within ~1 hour.
- It is probably not necessary to remove LET from the spacecraft to determine that it is functioning.

Issues and Concerns
(no particular order)

- L1 Detectors
- Schedule
  (detectors, VLSI, overall)
- Thermal Design
- Operational Heater Power
- Shielding – LET is more exposed
- Additional reporting requirements, coupled with already thin staffing
- Funding arrives irregularly, in small increments, requiring extra staff time